

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASA AKI KAMIYA,
KENJI AOKI and
NAOTO SAITO

Appeal No. 96-0161
Application 08/006,152¹

ON BRIEF

Before GARRIS, WEIFFENBACH and PAK, Administrative Patent Judges.
PAK, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the examiner's final
rejection of claims 1 through 28, which are all of the claims in
the application.

¹ Application for patent filed January 19, 1993. According to
applicants, this application is a continuation of Application 07/821,318,
filed January 13, 1992 (abandoned); which is a continuation of application
07/565,221, filed August 10, 1990 (abandoned).

Claim 1 is illustrative of the subject matter on appeal and reads as follows:

1. A method of producing a semiconductor device comprising:
 - a) forming a gate insulating film on a substrate at a surface of a semiconductor region of the substrate, the region being of a first conductivity type, and forming a gate electrode on the gate insulating film;
 - b) evacuating a chamber at a pressure of less than 1×10^{-4} Pa;
 - c) removing an inert film from the substrate in the chamber by a reduction reaction in order to expose an active face on two sections of the semiconductor region spaced from each other by the gate electrode;
 - d) applying to the surface of the substrate in the chamber a gas containing an impurity component of a second conductivity type while heating the substrate to a temperature greater than 800EC and not higher than a temperature of 825EC to form an impurity adsorption layer composed of impurity component atoms or of a compound containing at least impurity component atoms and constituting a diffusion source substantially only on the active face, and introducing the impurity component atoms into the semiconductor region of the first conductivity type from the diffusion source to thereby form a first impurity layer of low density in the surface of the two semiconductor region sections; and
 - e) forming a second impurity layer having an impurity density higher than that of the first impurity layer in each section so that the second layer is contiguous to the first impurity layer.

Appeal No. 96-01612
Application 08/006,152

As evidence of obviousness, the examiner relies on the following prior art:

Nickl	3,506,508	Apr. 14, 1970
Tsunashima et al. (Tsunashima)	4,791,074	Dec. 13, 1988 (Filed Jul. 15, 1987)
Schachameyer et al. (Schachameyer)	4,940,505	July 10, 1990 (Filed Dec. 2, 1988)
Ito (Japanese Kokai Patent Publication)	63-166220	July 9, 1988

Silicon Processing for the VLSI ERA, Vol. 1: Process Technology, Wolf et al., Lattice Press, Sunset Beach, California, 1986, pp 64-65 (hereinafter referred to as "Wolf").

Appellants' admission at pages 1 and 2 of the specification (hereinafter referred to as "admitted prior art").

Claims 1 through 28 stand rejected under 35 U.S.C. § 103 as unpatentable over the combined teachings of Tsunashima, Ito, Wolf, the admitted prior art and either Nickl or Schachameyer.

We reverse.

The subject matter on appeal is directed to "a method of producing a semiconductor device in the form of a metal insulator semiconductor field effect transistor (hereinafter, referred to as a "MISFET") used in electronic instruments such as computers." See specification, page 1, lines 1-8. The method initially involves removing an inert film from semiconductor regions of

Appeal No. 96-01612
Application 08/006,152

a substrate located adjacent to a gate electrode by a reduction reaction under a pressure of less than 1×10^{-4} Pa to provide an active face. See claims 1, 7, 23 and 24. An impurity adsorption layer composed of an impurity component atom of a second conductivity or of a compound containing impurity component atoms of a second conductivity is formed substantially only on the active face by applying a gas containing an impurity component on the active face as the silicon substrate is heated between 800 and 825°C. Id. The impurity component is introduced into the semi-conductor regions of the first conductivity using the impurity adsorption layer as a diffusion source. Id.

In rejecting the appealed subject matter under 35 U.S.C. § 103, the examiner takes the position that it would have been obvious to remove an inert film from particular regions of a silicon substrate as taught by Tsunashima using the high vacuum hydrogen (reducing) etching technique taught by either Nickl or Schachameyer and then provide an impurity on the resulting active face area as taught by Tsunashima using the chemical deposition technique as taught by Ito. See Answer at pages 4-6. The examiner relies on the admitted art for showing that "making LDD and DDD devices are conventional in semiconductor processing and that ion implantation is not an efficient method of forming a

shallow junction." See Answer at page 5. The examiner relies on Wolf to show "the equivalence among dopants" See Answer at page 6.

For the reasons well articulated by appellants in the "argument" section of their Brief at pages 13 through 24, we cannot subscribe to the examiner's reasoning. Suffice to say that the examiner has not established that the prior art as a whole would have suggested to one of ordinary skill in the art a combination of exposing an active face on semiconductor regions of a substrate, which are spaced from each other by a gate electrode, by a reduction reaction and then forming an impurity adsorption layer substantially only on the active face using a chemical vapor deposition technique. For example, the examiner's position is contrary to the teaching of Tsunashima which directs away from forming an impurity adsorption layer substantially only on the active face. See Brief at page 13 in conjunction with Tsunashima at column 4, lines 2-4. The examiner has not supplied any evidence that the semiconductor device of the type described in Tsunashima can be made by forming an impurity adsorption layer substantially only on the active face after the active face is exposed by a reduction reaction.

Appeal No. 96-01612
Application 08/006,152

The decision of the examiner is reversed.

REVERSED

BRADLEY R. GARRIS)	
Administrative Patent Judge)	
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CAMERON WEIFFENBACH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
)	
CHUNG K. PAK)	
Administrative Patent Judge)	

Appeal No. 96-01612
Application 08/006,152

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