

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN C. McMAHAN, KENNETH C. SCHEUER,
WILLIAM B. LEDBETTER, Jr.,
MICHAEL G. GALLUP and JAMES G. GAY

Appeal No. 95-4154
Application 08/122,193¹

ON BRIEF

Before JERRY SMITH, LEE and CARMICHAEL, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 30-40, 43 and 45. Claims 41-42 and 44 have been objected to. No claim has been allowed.

¹ Application for patent filed September 15, 1993. According to the appellants, it is a continuation of Application 07/931,187, filed August 17, 1992, now Patent No. 5,294,845, which is a continuation of Application 07/632,901, filed December 24, 1990, now Patent No. 5,162,672.

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References relied on by the Examiner

Asano et al. (Asano)	4,719,369	Jan. 12, 1988
Anderson	5,039,874	Aug. 13, 1991 (filed Mar. 15, 1990)

The Rejections on Appeal

Claims 30, 31 and 35-37 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Asano.

Claims 32, 33 and 43 stand finally rejected under 35 U.S.C. § 103 as being unpatentable over Asano and Anderson.

Claims 34, 38, 39, 40 and 45 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. § 103 as being unpatentable over Asano.

Claims 30, 38 and 43 are the only independent claims.

The Invention

The invention is directed to an integrated circuit having a plurality of output buffers each with an output coupled to the output terminal of the integrated circuit. Each output buffer is coupled between the input terminal of the integrated circuit and the output terminal in response to a control signal which is varied in response to an impedance selection input asserted at an input pin of the integrated circuit. A user can select

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predetermined discrete output impedances of the circuit by controlling the value of the impedance selection input.

Representative claim 30 is reproduced below:

30. In an integrated circuit, a circuit having an output terminal, comprising:

a plurality of output buffers, each output buffer having a predetermined buffer output impedance, an input coupled to a buffer information input terminal of the circuit, and an output coupled to the output terminal of the circuit, each output buffer being electrically coupled between the information input terminal and the output terminal in response to a control signal having a value which is controlled and may be varied only during a predetermined mode of operation of the integrated circuit by a user of the circuit in response to an impedance selection input being asserted at an input pin of the integrated circuit, the user being able to select predetermined discrete, output impedances of the circuit by controlling the value of the impedance selection input.

Claims 30 and 43 require that the control signal be varied or modified only during a predetermined mode of operation of the integrated circuit.

Claim 38 requires that the user is able only during reset of the integrated circuit to select predetermined discrete, output impedances of the circuit.

Claim 43 further requires that the control signal be stored.

Opinion

Anticipation is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of the claimed invention. In

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re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Each of independent claims 30, 38 and 43 specifically provides for user selection of "predetermined discrete, output impedances" of the integrated circuit by either controlling or inputting a select input or impedance selection input to an input pin of the circuit. We agree with the appellants that Asano does not disclose user selection of "predetermined discrete, output impedances" of the integrated circuit.

The examiner relies on the input A and resistor 22 shown in Asano's Figure 2 as an impedance selection input (answer at 3, lines 9-13). However, as is described in Asano from column 3, line 57, to column 4, line 32, the user selection of a value for resistor 22 and a value for input A only causes the plurality of output transistors 1-5 to be selectively turned on or off during operations over the whole range of the drain current of the monitoring transistor 20. In column 4, lines 24-32, Asano states:

As a result, the output resistor of the output circuit can be rendered to match the characteristic impedance of the transmission line by controlling the gate width of the output transistors turned on in accordance with the magnitude of the drain current within the control range of the element production variations. The

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control circuit 25 may be configured the same way as the control circuit 24 but with different polarities of the control signal 27.

The appellants correctly assert (Br. at 5, lines 31-33) that in Asano, the selection of the input A merely calibrates the range of control values to correspond to the full range of the drain current of the monitoring transistor 20. Precisely what output impedance the circuit will have depends on the detected drain current during operation. The appellants are correct that such functionality of Asano does not allow the user to "select predetermined discrete, output impedances of the circuit" (Br. at 5, lines 23-25). The objective of Asano is to automatically match the output resistance of the circuit with the impedance of the transmission line (column 2, lines 43-45), not to have user selection of predetermined discrete, output impedances.

We decline to read the claim language on user selection of "predetermined discrete, output impedances of the circuit" so broad as to cover the case of having a number of possible impedance values based on another parameter over which the user does not control, i.e., the drain current of Asano's monitoring transistor 20. In the context of the appellants' specification, "select" means choosing a particular value or setting. The language of selecting predetermined discrete output impedances

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reasonably means only the selection of one particular impedance value among a plurality of selectable values as the output impedance, not a plurality of impedance values any one of which may ultimately turn out to be the actual output impedance depending on something over which the user does not control.

While features not claimed should not be read into the claims from the specification, claim terms also must be interpreted reasonably in light of the specification. The appellants' disclosed invention and specification concern the causing of the circuit to exhibit a specific impedance known to the user. In our view, it would not be consistent with the specification to interpret the claims as reading on something which defines a range or plurality of impedance values over which the actual output impedance will vary based on the characteristic impedance of the transmission line or the drain current of a monitoring transistor.

Additionally, Asano does not disclose when input A is provided by a user, assuming that the input A is provided by a user. It would be mere speculation to assume that the input A is provided only during a predetermined mode of operation or only during reset. Nothing precludes inputting the A signal at some other time.

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For the foregoing reasons, the rejection of claims 30, 31 and 35-37 as being anticipated by Asano cannot be sustained. The rejection of claims 34, 38, 39, 40 and 45 also cannot be sustained.

Regarding the rejection of claims 34, 38, 39, 40 and 45 under 35 U.S.C. § 103 as being unpatentable over Asano, the examiner has articulated no motivation for one with ordinary skill in the art to eliminate the monitoring transistor 20 in Asano and to have a user enter a specific selection of one output impedance to be exhibited by the integrated circuit. The mere fact that the prior art may be modified in a manner to yield the claimed invention does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992). Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor. Para-Ordnance Mfg., Inc. v. SGS Importers Int'l, Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995).

Thus, we do not sustain the obviousness rejection of claims 34, 38, 39, 40 and 45 over Asano.

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Regarding the rejection of claims 32, 33 and 43 under 35 U.S.C. § 103 as being unpatentable over Asano and Anderson, Anderson has been relied on only to show the "storage" aspect of those claims and would not make up for the deficiency of Asano as already discussed in connection with the anticipation rejection and the obviousness rejection over Asano.

Accordingly, we do not sustain the obviousness rejection of claims 32, 33 and 43 over Asano and Anderson.

Conclusion

The rejection of claims 30, 31 and 35-37 under 35 U.S.C. § 102(b) as being anticipated by Asano is reversed.

The rejection of claims 32, 33 and 43 under 35 U.S.C. § 103 as being unpatentable over Asano and Anderson is reversed.

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The rejection of claims 34, 38, 39, 40 and 45 under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103, as being unpatentable over Asano is reversed.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
JAMESON LEE)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
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