

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIDEO ARAI, KEIZO NISHIMURA
and YASUYUKI INOUE

Appeal No. 95-3916
Application 08/008,292¹

HEARD: September 16, 1997

Before HAIRSTON, BARRETT, and FLEMING, Administrative Patent
Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed January 25, 1993. According to applicants, the application is a continuation of Application 07/551,009, filed July 11, 1990.

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This is an appeal from the final rejection of claims 26 through 28 and 30 through 36. In an Amendment After Final (paper number 12), claims 26 through 28 and 30 through 32 were amended.

The disclosed invention relates to a code error correction method and apparatus for decoding a digital information signal comprised of a set of code blocks.

Claim 26 is illustrative of the claimed invention, and it reads as follows:

26. A code error correction apparatus for decoding a digital information signal comprised of a set of code blocks, said digital information signal being received at least twice by repetitive transmissions or repetitive reproductions of original data, comprising:

error correction means for sequentially error-correcting a set of code blocks of each digital information signal on a code block basis, said error correction means providing a set of error flags each representing whether or not the corresponding code block is an uncorrected code block after error correction;

check information generation means for generating a check information code for each of the code blocks after error correction of a digital information signal, to thereby provide a set of check information codes for each digital information signal;

memory means having a memory capacity to store a set of code blocks of one digital information signal and at least a set of check information codes of said one digital information signal and a set of check information codes of a subsequent digital information signal, a same code block of different digital information signals being stored in a predetermined same memory location;

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error flag memory means for storing the set of error flags of said subsequent digital information signal on a code block basis;

control means for controlling a read/write operation to said memory means and said error flag memory means; and

check means for comparing a set of check information codes of said one digital information signal with a set of check information codes of said subsequent digital information signal both stored in said memory means, on a check information code basis;

wherein said control means writes correct code blocks and corrected code blocks after error correction of said one digital information signal at respective memory locations of said memory means as well as the check information codes thereof in view of the set of error flags stored in said error flag memory means for said one digital information signal;

said control means then writes correct code blocks and corrected code blocks after error correction of said subsequent digital information signal at respective memory location of said memory means as well as the check information codes thereof in view of the set of error flags stored in said error flag memory means for said subsequent digital information signal, and

said control means sets error flags for same code blocks of said one and subsequent digital information signal in said error flag memory means, where the error flags for both the same code blocks stored in said error flag memory means indicate that the same code blocks are correct or corrected code blocks, but a comparison result by said check means indicates that the check information codes of both the same code blocks do not coincide with each other.

The references relied on by the examiner are:

Takagi et al. (Takagi)	4,742,517	May 3, 1988
Preissler	4,918,694	Apr. 17, 1990

Claims 26 through 28 and 30 through 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Preissler.

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Claims 33 through 36 stand rejected under 35 U.S.C. § 103 as being unpatentable over Preissler and Takagi.

Reference is made to the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 26 through 28 and 30 through 36.

According to the examiner (Answer, page 3)

Preissler discloses the invention substantially as claimed. Preissler discloses that a system for correcting data has an inner decoder which determines whether or not the data is uncorrectable and the inner decoder provides an error flag thereafter. The data is then put into a buffer memory (2). Later, this data is read out under the control of a control circuit (3) and is supplied to a comparison circuit (8) (figure 2, column 3 lines 39-64).

In rebuttal to appellants' argument (Brief, page 7) that "Appellants' invention differs from Preissler being that in Appellants' invention error free code blocks themselves are not compared but check information codes are compared instead," the examiner indicates (Answer, page 8) that

[a]lthough Preissler does not use the specific phrase "comparing the check information codes", Preissler teaches that check words are added in the recording of the data words (column 1 lines 37-38). Preissler also teaches that the data words are compared by a comparison circuit (8). The feature of comparing the

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check information codes is inherent in the operation of Preissler's comparison. This is because when data words are compared by comparison circuit of Preissler, the check words (which added to the data words) are compared as well.

In response to the examiner's contentions concerning the teachings of Preissler, appellants argue (Reply Brief, pages 4 to 5) that

[i]n column 3, lines 39-64 of Preissler, Preissler specifically teaches that the read control circuit 3 reads out data of a first and a second recording in a time multiplex manner from storage 2. Preissler further teaches that at one time four bits of audio data and one error flag bit is read out for each of the first and second recordings and supplied to the registers 6, 7 and 4, 5 respectively. In Preissler based on clocking provided by the control circuit 3, ten bits of data (four bits audio data and one bit error flag for each of the first and second recordings) are made available from the combination of registers 5 and 7 with the two, four bit parallel audio data portions being supplied to the comparison circuit 8 and the two parallel one bit error flag data being supplied to the OR gate 9. The comparison circuit 8 compares the two parallel four bit audio data so as to output a signal to OR gates 10 and 11. The two parallel one bit flag data provided to the OR gate 9 causes the OR gate 9 to output a signal which enables the operation of the comparison circuit 8 when the error flag has been set in any one of the two parallel one bit error flag data. Preissler clearly teaches that the comparison circuit 8 is active (enabled) only when neither of the audio data portions is accompanied by an error flag.

Appellants' assessment of the teachings of Preissler is correct. Thus, we agree with appellants (Reply Brief, pages 5 and 6) that the comparator 8 in Preissler merely compares audio

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data portions (i.e., the data words of first and second blocks), and not check information codes as recited in all of the claims on appeal. The obviousness rejection of claims 26 through 28 and 30 through 36 is reversed because the secondary reference to Takagi does not cure this shortcoming in the teachings of Preissler.

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DECISION

The decision of the examiner rejecting claims 26 through 28
and 30 through 36 under 35 U.S.C. § 103 is reversed.

REVERSED

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KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	
Administrative Patent Judge)	APPEALS AND
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)	INTERFERENCES
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MICHAEL R. FLEMING)	
Administrative Patent Judge)	

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