

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ERIK L. HEDBERG
and GARRETT S. KOCH

Appeal No. 95-3658
Application 07/777,877¹

ON BRIEF

Before HAIRSTON, BARRETT, and FLEMING, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

¹ Application for patent filed October 16, 1991, entitled "Method And Apparatus For Real Time Two Dimensional Redundancy Allocation."

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-8, 10-12, and 16-17, all of the claims pending in the application. Claims 9, 13-15, and 18-19 have been cancelled. The amendment received December 27, 1994 (Paper No. 12), has been entered and deemed to overcome the rejection under 35 U.S.C. § 112, second paragraph (Supp. Examiner's Answer, Paper No. 14, page 1).

The invention is directed to a memory array built in self test (ABIST) system for allocation of spare or redundant column lines and row lines for unacceptable memory array column and row lines. As disclosed, the ABIST is located on the semiconductor chip with the memory array. The ABIST has a first number of registers equal to the number of redundant columns and a second number of registers equal to the number of redundant rows. The columns are scanned sequentially and if more defects are found in the rows of a column than there are redundant rows, that column address is stored or "locked in" to the register for replacement. The rows are then scanned and columns whose addresses are in the first registers are masked. Rows with defects in the visible column locations have addresses "locked in" to the row registers until the number of row registers are filled and then any remaining empty column registers are used to store the column address of the defect. The column and row addresses are scanned out and a redundancy processor substitutes appropriate redundant column or row lines for faulty array column or row lines.

Claim 1 is reproduced below.

1. An array built in self test (ABIST) system comprising

a single semiconductor chip,

a memory array disposed on said semiconductor chip having a plurality of column lines and a plurality of row lines and at least one redundant column line and at least one redundant row line with cells coupled to the lines at intersections thereof,

first means coupled to said memory array for identifying a given number of faulty cells along each of said column lines,

first register means disposed on said semiconductor chip having a number of registers equal to the number of redundant column lines,

means for applying column address signals to said first register means,

means coupled to said first identifying means for storing the address signals of each of the column lines having said given number of faulty cells in said first register means,

second means coupled to said memory array for identifying a faulty cell along each of said row lines while masking the faulty cells having address signals of said column lines stored in said first register means,

second register means disposed on said semiconductor chip having a number of registers equal to the number of redundant row lines,

means for applying row address signals to said second register means,

means coupled to said second identifying means for storing the address signals of each of the row lines having a faulty cell in said second register means until said second register means is filled to capacity and then storing the column line address signals of any additional faulty cells identified in said row lines in said first register means, and

means coupled to said registers for substituting said redundant column and row lines for the column and row lines having address signals stored in said first and second register means.

The examiner relies on the following references:

Eaton, Jr. et al. (Eaton) 4,389,715 June 21, 1983
Harns 4,460,997 July 17, 1984

Harns discloses a memory tester for testing chips having a memory array with redundant rows and columns. As shown in figure 1, a memory device under test (DUT) is connected to a pin electronics and error detection board 14. A programmable pattern generator 25 provides address, clock, and signals for comparison for exercising and testing the memory DUT. An error capture and analysis system 31 (figure 2) provides memory repair analysis capability and has two main modes of operation described at column 5, lines 16-49. In a first test mode, the DUT 13 is tested under programmable pattern generator 25 control and the resultant failure data is stored in a bit fail random access memory (BFRAM) 49. The BFRAM 49 is configured to correspond to one of the different memory matrix configurations under test (column 6, lines 33-36). In a second mode of operation, post processing logic circuit 70 in system 31 processes the error data to determine the repairability of the memory DUT as described at column 5, lines 23-49 and column 18, line 50 to column 19, line 14. "The post processing logic circuit includes a row mask ram and a column mask ram which stores the addresses of rows and columns which are masked for replacement" (column 9, lines 61-64; see also column 14, lines 16-22).

Eaton discloses a RAM with spare rows and columns of memory cells to provide redundancy. The RAM includes a plurality of address buffers. Associated with each buffer is a store for a defective row

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address, a store for a defective column address, and a comparator. "The stores retain defective memory cell addresses which the comparator sequentially compares against the address data sequentially output by the buffer. When the comparator senses a match, a control signal is generated to initiate substitution of spare memory cells for the defective main memory cells." (Abstract.)

Claims 1-8, 10-12, and 16-17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Harns and Eaton. The examiner finds that "Harns does not teach having a first and second register to hold the address of the faulty row/columns located on the same chip as the memory array" (Final Rejection, page 2; see also Examiner's Answer, page 3). The examiner finds that Eaton discloses storing the defective row and column addresses in stores on the same chip as the memory array and concludes that this would have suggested to the artisan placing memory failure registers on the same chip as the memory array (Final Rejection, page 2; Examiner's Answer, page 3).

OPINION

We affirm-in-part.

The level of ordinary skill is not argued, so we find the references to be representative of the level of skill in the art. See In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"). Cf. Chore-Time Equipment Inc. v. Cumberland Corp., 713 F.2d 774, 779 n.2, 218 USPQ 673, 676 n.2 (Fed. Cir. 1983) ("We hold only that an invention may be held to have been obvious (or nonobvious) without a specific finding of a particular level of skill in the art where, as here, the

prior art itself reflects an appropriate level and a need for such expert testimony has not been shown."). Those of ordinary skill in the art must also be presumed to know something about the art apart from what the references expressly disclose. In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962).

Claims 1 and 8

Initially, we analyze and interpret claim 1.

Claim 1 is an open ended claim because of the transition word "comprising" and does not exclude the presence of other structure in the applied prior art, such as the second matrix memory BFRAM 49 in Harns.

While the examiner finds a difference in the order of testing the rows and columns and concludes that the order is a matter of design choice (Examiner's Answer, page 4), Harns expressly discloses that rows and columns are interchangeable (column 30, lines 43-52). Thus, the order is not a difference.

The "array built in self test (ABIST) system" in the preamble of claim 1 does not require all means in the body of the claim to be disposed on the chip. Compare this to claim 2 which expressly recites an "array built in self test (ABIST) system disposed on a single semiconductor chip" (emphasis added). In claim 1, the "first means coupled to said memory array for identifying" (emphasis added) does not require the first identifying means to be on the chip; it could be external circuitry coupled to the memory array through pins or a probe. The same is true for the second identifying means. Nor does claim 1 require the "means for applying column address signals," "means . . . for storing the address signals . . . in said first

register means," "means for applying row address signals," and "means . . . for storing the address signals . . . in said second register means until said second register means is filled to capacity and then storing the column line address signals . . . in said first register means" to be on the chip. Only the memory array and the first and second register means are expressly claimed as being "disposed on said semiconductor chip."

Importantly, claim 1, as interpreted, does not require the column and row address signals to be stored or "locked in" as the column and rows are being tested. The claimed "means . . . for storing the address signals" does not state when the address signals are stored, which broadly leaves open the interpretation that the address signals can be stored in the on-chip registers after the testing is all complete (as in Eaton). The "means coupled to said registers for substituting said redundant column and row lines" is not limited to laser fuse blowing circuitry which blows fuses in response to addresses stored in the registers as disclosed (e.g., specification, page 8) and broadly encompasses circuitry for substituting column and row lines in response to the stored addresses (e.g., the spare column decoder and spare row decoder circuitry in Eaton which accesses spare columns and spare rows). Claim 1 does not capture the "real time" aspect of the disclosed circuitry where the logic circuitry cooperates with the registers and the data comparison circuitry to lock the addresses into the registers during testing.

The examiner finds that Eaton discloses storing the defective row and column addresses in stores on the same chip as the memory array and concludes that this would have suggested to the artisan placing memory failure registers on the same chip as the memory array (Final Rejection, page 2; Examiner's

Answer, page 3). We agree. The examiner's response to the arguments confuses rather than simplifies the rejection in terms of what modification is being proposed and will be discussed later.

Eaton describes that the addresses of defective main rows and column lines are stored or programmed in fuse circuitry in the RAM during probe testing (e.g., column 2, line 62 to column 3, line 6). This circuitry is equivalent to the claimed first and second register means because it stores addresses electronically. Structures in Harns and Eaton that perform the claimed functions are presumed to be equivalent to structures disclosed to correspond to the claimed means under 35 U.S.C. § 112, sixth paragraph, absent argument to the contrary. See Examination Guidelines for Claims Reciting a Means or Step Plus Function Limitation In Accordance With 35 U.S.C. § 112, 6th Paragraph, 1162 Off. Gaz. Pat. & Trademark Office 59, 59-60 (May 17, 1994) (Guidelines). Manifestly, Eaton must have structure for applying the column and row addresses from the testing system to the address stores. The spare column decoders (SCD) and spare row decoders (SRD) in Eaton are coupled to the address storing circuitry and function to substitute spare columns and spare rows (column 2, line 62 to column 3, line 19). Thus, the SCD and SRD and their accompanying circuitry in Eaton constitute "means coupled to said registers for substituting said redundant column and row lines" (claim 1). Harns has column and row mask RAMs 171 and 172 that hold the addresses of columns and rows selected for replacement according to the broad algorithm recited in claim 1. It would have been obvious to the artisan to substitute a chip such as Eaton for the memory DUT in Harns and to store the addresses of defective columns and rows from Harns in the chip address circuitry because such chips require the addresses of defective columns and rows so that

substitution of columns and rows will be transparent. Stated differently, it would have been obvious to test and program a chip with address registers such as Eaton with the testing system of Harns because Harns is not limited to testing any particular type of memory device. The rejection does require physically shifting structure from the test system of Harns on to the memory DUT.

For the reasons stated above, it is our opinion that a prima facie case of obviousness has been established with respect to claim 1 and also with respect to claim 8, which is of the same scope because the limitations of first and second pluralities of lines arranged orthogonally to each other is met by the columns and rows shown in Harns.

Appellants argue that they "store addresses of failing lines in registers and not the bit location of a failed cell in a second memory array" (Brief, page 9). Appellants assume that it is structure corresponding to the BFRAM of Harns that the examiner proposes putting on the same semiconductor chip as the memory (Brief, pages 9-10). However, the statements of the rejection in the Final Rejection and in the Examiner's Answer discuss "registers" and "memory failure registers," generally, not the BFRAM. Harns has column and row mask RAMs 171 and 172 that hold the addresses of columns and rows selected for replacement and these RAMs correspond most closely to the first and second register means except that they are not on the chip. The address replacement information in the RAMs of Harns is the information that would be stored in the address circuitry of the memory chip of Eaton. It is not reasonable to consider the BFRAM to be the row and column registers that are proposed to be mounted on the chip because: (1) the BFRAM holds an image of the failure data, not addresses of the results of the row and column

replacement algorithm on the failure data; (2) the BFRAM is structurally different from the address circuitry in Eaton which is the structure the rejection proposes to be on the chip.

The examiner's response to the arguments (Examiner's Answer, pages 4-6) confuses rather than clarifies the rejection. We have addressed the rejection as we understand it from the statement of the rejection. We understand that the disclosed and claimed invention stores addresses of failed rows and columns, not locations of stored cells (Reply Brief, pages 2-5). However, Harns discloses storing both the location of stored bits in the two-dimensional BFRAM and the address of failed rows and columns in RAMs 171 and 172. Appellants do not address the teaching of identifying defective columns and rows in Harns. The examiner discusses that appellants' invention stores the address of the faulty cells in a two dimensional failed address register and since the BFRAM is a two dimensional array this suggests that the examiner proposes putting a BFRAM structure on the chip. It appears that the examiner may have been confused by appellants' arguments about the BFRAM. The fact is that Harns identifies the addresses of columns and rows selected for replacement in the same manner as the disclosed invention and the rejection is that it would have been obvious to store these defective addresses in registers on the chip as taught by Eaton. The fact that Harns uses a BFRAM to hold an image of the faulty cells as intermediate structure in the test system for identifying faulty columns and rows is not precluded by claim 1.

Appellants discuss the structure disclosed in the specification corresponding to the various means of claim 1 (Brief, page 11). However, appellants do not raise the question of claim interpretation under 35 U.S.C. § 112, sixth paragraph. We presume that the structures in Harns and Eaton that perform the

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claimed functions are equivalent under 35 U.S.C. § 112, sixth paragraph, absent argument to the contrary. See Guidelines, 1162 Off. Gaz. Pat. & Trademark Office at 59-60. Limitations of the disclosed structure are not read into the claims. For example, although the first identifying means is disclosed to be a data compression circuit on the chip the claim recites only that the first identifying means is "coupled to said memory array," which does not require the means to be on the chip.

Appellants argue (Brief, pages 11-12):

Neither Harns nor EAton [sic], Jr., et al, nor the combination thereof, teach a test system located on the same semiconductor chip with the device or memory under test wherein column addresses are applied to a register located on the memory chip and stored or locked therein when means identify a given plurality of faulty cells along a given column line and row addresses are applied to another register also located on the same chip and stored or locked therein when means identify a faulty cell when scanning the memory along a given row.

Claim 1 does not require the whole test system to be located on the same semiconductor chip. Only those means expressly recited to be on the chip are required to be on the chip, i.e., the memory array and the first and second register means. Claim 1 also does not recite locking an address into a register when (in the time sense of immediately after) means identify a given number of faulty cells as suggested by appellants' argument. The claimed "means . . . for storing the address signals" could store the addresses after the whole testing process is finished, although this interpretation is not at issue.

Appellants' arguments do not rebut the prima facie case of obviousness. Accordingly, the rejection of claims 1 and 8 is sustained.

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Claims 2-7, 10, and 16

Claims 2-7 require an "array built in self test (ABIST) system disposed on a single semiconductor chip" (emphasis added) and claims 10 and 16 require a "built in self test system formed on a semiconductor chip" (emphasis added). These limitations require all the structure recited in these claims to be disposed on the chip. Harns is not an ABIST system on the same chip as the device to be tested and the examiner has not cited an ABIST reference. The examiner's only motivation for putting the test system of Harns on the chip is that changes in semiconductor technology allow a designer to put more circuitry on a chip (Examiner's Answer, page 3). We agree with appellants' arguments (Brief, page 10) that there is no logical motivation to put the test system of Harns on the same chip as the memory device because that would require putting a BFRAM as large as the memory under test on the chip, doubling the size of the memory just for the test circuitry. Furthermore, because the BFRAM would not have been tested it would be unsuitable for use as part of a testing system, that is, the BFRAM memory would have to be tested before the memory array itself could be tested. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1982), citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). There is no suggestion in the applied references for putting the test circuitry on the same chip as the memory array. Nor would putting the circuitry on the same chip produce a practical device. Accordingly, the rejection of claims 2-7, 10, and 16 is reversed.

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Claims 11, 12, and 17

Claim 11 is more detailed than claim 1 and recites specific elements and their relationship to one another. The examiner states that "appellant has not stated which elements of the claim are not clearly taught by the combination of Harns and Eaton" (Examiner's Answer, page 8) and "asserts that Harns and Eaton teach the claimed elements (as described above in paragraph 9) and that the timing relationships claimed are equivalent to that disclosed in Harns" (Examiner's Answer, page 8). Claim 11 is more detailed than claim 1 and the correspondence of elements and relationships to Harns is not clear to us as it was with claim 1. It is the examiner's responsibility to establish a prima facie case that the claimed subject matter is unpatentable and we conclude this has not been done with respect to claim 11. Accordingly, the rejection of claims 11, 12, and 17 is reversed.

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CONCLUSION

The rejection of claims 1 and 8 is sustained.

The rejection of claims 2-7, 10-12, and 16-17 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| KENNETH W. HAIRSTON |) | |
| Administrative Patent Judge |) | |
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| |) | BOARD OF PATENT |
| LEE E. BARRETT |) | APPEALS |
| Administrative Patent Judge |) | AND |
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