

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 36

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUN-ICHI NISHIZAWA

Appeal No. 95-3573
Application No. 07/839,704¹

ON BRIEF

Before HAIRSTON, JERRY SMITH and BARRETT, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 31 through 37, 41 through 69, 86 and 87.

¹ Application for patent filed February 24, 1992. According to the appellant, the application is a continuation of Application No. 07/428,897, filed October 30, 1989, now abandoned, which is a continuation of Application No. 07/087,974, filed August 17, 1987, now abandoned, which is a continuation of Application No. 06/514,594, filed July 18, 1983, now abandoned, which is a continuation of Application No. 06/174,725, filed August 1, 1980, now U.S. Patent No. 4,434,433, which is a continuation of Application No. 05/878,441, filed February 16, 1978, now abandoned.

The disclosed invention relates to a semiconductor memory cell array that comprises a semiconductor body, a plurality of bit lines and a plurality of word lines crossing the bit lines to form a matrix, and at least one semiconductor memory cell disposed in the semiconductor body at each crossing of the bit lines and the word lines.

Claim 45 is illustrative of the claimed invention, and it reads as follows:

45. A semiconductor memory cell array comprising:

a semiconductor body, a plurality of bit lines and a plurality of word lines crossing said bit lines to form a matrix and at least one semiconductor memory cell disposed at one of the cross points of said bit lines and word lines, said semiconductor memory cell including:

a source region formed with a low resistivity semiconductor region of a first conductivity type for supplying and retrieving charge carriers;

a storage region formed with a semiconductor region of said first conductivity type and disposed separate from said source region and constituting one electrode of a capacitor for storing signal charge;

means for forming the other electrode of said capacitor;

a channel region formed with a high resistivity semiconductor region of said first conductivity type disposed between said source region and said storage region and adapted for forming a controllable current path for charge carriers therebetween, said source, channel, and storage regions being disposed in said semiconductor body;

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gate means disposed in the neighborhood of said channel region and substantially surrounding and defining said channel regions and forming a pn junction therewith for controlling the potential distribution in said channel region;

said pn junction forming a depletion layer extending into said channel region to at least nearly pinch-off said channel region in the absence of bias voltage applied to said gate region wherein said depletion layer is controllable by the voltage applied to said source region with respect to said other electrode forming means;

said source and said storage regions are aligned substantially perpendicular to the surface of said semiconductor body;

one of said source and said storage regions is disposed in the neighborhood of the surface of said semiconductor body and the other of said source and said storage regions is disposed in the bulk of said semiconductor body.

The references relied on by the examiner are:

Ishitani	3,982,264	Sept. 21, 1976
Cade	3,986,180	Oct. 12, 1976
Schuermeyer et al. (Schuermeyer)	4,064,492	Dec. 20, 1977
Jenne	4,105,475	Aug. 8, 1978
	(effective filing date	Oct. 23, 1975)
Harari	4,115,914	Sept. 26, 1978
	(effective filing date	Mar. 26, 1976)

Clarke et al. (Clarke), Capacitor for Single FET Memory Cell, IBM Technical Disclosure Bulletin, Vol. 17, No. 9, February 1975, pages 2579 and 2580.

Junction Field-Effect Transistor Designed for Speedy Logic, Electronics International Edition, August 19, 1976, pages 4E and 6E.

Claims 86 and 87 stand rejected under the first and second paragraphs of 35 U.S.C. § 112 for lack of enablement and for indefiniteness.

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Claim 57 stands rejected under the fourth paragraph of 35 U.S.C. § 112 as being of improper dependent form by failing to further limit the subject matter of previous claim 55.

Claims 31 through 33, 36, 37, 41, 45 through 55, 57 through 61, 63, 64, 68 and 69 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cade in view of Jenne and the Electronics publication.

Claims 58, 59, 63, 64 and 68 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cade in view of Jenne.

Claims 31 through 37, 41, 55 through 61, 63, 64, 68 and 69 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cade in view of Jenne, the Electronics publication and Clarke.

Claims 31 through 33, 36, 37, 41 through 43, 55, 57 through 68 and 69 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cade in view of Jenne, the Electronics publication and Ishitani.

Claims 31, 32, 36, 37 and 44 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cade in view of Jenne, the Electronics publication, Schuermeyer and Harari.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

OPINION

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We have carefully considered the entire record before us, and we will reverse all of the rejections.

In the non-enablement and indefiniteness rejections of claims 86 and 87, the examiner states (Answer, page 5) that:

It is not seen where or how the "further" transistor of claim 86 is supposed to be related to the memory cell of claim 36. Note that, while applicant has made reference to Figs. 20a-20c here, . . . whatever these vague figures were intended to mean, which cannot be understood, in any case it is clear that these figures were an alternative to, and not a combination with, the memory cells otherwise claimed here. Figs. 20a-20c most certainly do not support these claims.

We agree with appellant's argument (Brief, pages 25 and 26) that:

We point out that in lines 20-23, page 37 of the specification, a memory cell as presently claimed is described as being connected with a sensor. FIGS. 20A-20C . . . depict a combination of the claimed sensor with a generic memory cell, not a *sensor unit* which incorporates a memory device.

Accordingly, we disagree with the examiner that "these figures [20A through 20C] were an alternative to, and not a combination with, the memory cells otherwise claimed here." The rejections of claims 86 and 87 under the first and second paragraphs of 35 U.S.C. § 112 are reversed because the examiner has not demonstrated that the skilled artisan would not have known how to make and or use the disclosed and claimed invention without undue experimentation, and that the claimed invention is indefinite.

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In response to the examiner's rejection of claim 57 under the fourth paragraph of 35 U.S.C. § 112 as being redundant with claim 55, appellant argues (Brief, page 25) that "'connected' in claim 55 may be interpreted to refer to any type of connection," and that "'electrically connected' in claim 55 is a properly recited further limitation." We agree. The rejection of claim 57 under the fourth paragraph of 35 U.S.C. § 112 is reversed.

Appellant's response to the prior art rejections of the claims on appeal is an argument (Brief, pages 3, 11 and 21, and second Reply Brief, pages 1 and 2) that none of the applied references shows a pn junction that forms a depletion layer extending into the channel region to "at least nearly" pinch-off² the channel region in the absence of a bias voltage applied to the gate region. We agree. Cade clearly indicates (column 8, lines 8 through 18) that the entire channel region is completely pinched-off, and the Electronics publication merely states that the transistor is "cut off." Thus, all of the obviousness rejections are reversed because Ishitani, Schuermeyer, Jenne,

² All of the independent claims on appeal either recite that a depletion layer is formed extending into the channel region to "at least nearly pinch-off" the channel region, or that a potential distribution forms a potential barrier "which approaches a pinch-off."

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Harari and Clark do not cure the noted shortcoming in the teachings of Cade and the Electronics publication.

DECISION

In view of the reversal of all of the rejections of record, the decision of the examiner is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
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)	
)	BOARD OF PATENT
JERRY SMITH)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
LEE E. BARRETT)	
Administrative Patent Judge)	

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Serial No. 07/839,704

Judge HAIRSTON

Judge JERRY SMITH

Judge BARRETT

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DECISION: REVERSED

Send Reference(s): Yes No
or Translation(s)

Panel Change: Yes No

3-Person Conf. Yes No

Heard: Yes No

Remanded: Yes No

Index Sheet-2901 Rejection(s): _____

Acts 2: _____

Palm: _____

Mailed:

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