Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LEE A. CHRISTEL and THEODORE J. VERMEULEN

Appeal No. 1995-3557
Application No. 07/833,417[1]

ON BRIEF

Before KIMLIN, OWENS, and SPIEGEL, *Administrative Patent Judges*.

SPIEGEL, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1 through 18, which are all of the claims pending in this application. Claims 1, 2 and 10 through 18 are illustrative and are appended to this decision.

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[1] Application for patent filed February 10, 1992.

Appellants' claimed invention is directed to a method of micromachining silicon to form a buried boss diaphragm structure having relatively thick boss sections and relatively thin flexure sections and the product made thereby. The method comprises (1) providing a substrate of a first type (p-type) doped silicon, which can be attacked by a selected etchant material, (2) deeply diffusing a second type (n-type) dopant only into selected areas on a surface of the first type doped silicon where the boss sections are to be formed (thus defining areas of the first type doped silicon which cannot be attacked by the selected etchant material) and only to a depth (x-y) less than the desired thickness (x) of the boss diaphragm structure, (3) growing an epitaxial layer of second type (n-type) doped silicon (which also cannot be attacked by the selected etchant material) to a desired flexure section thickness (y) over the same surface of the substrate that has been diffusion doped, and then (4) etching away the first-type (p-type) doped silicon so to leave the relatively thick boss sections joined by the relatively thin flexure sections, thus forming a boss diaphragm structure of desired thickness (x).

The examiner relies upon the following references as evidence of obviousness:

Wise et al. (Wise)	5,059,543	Oct. 22, 1991
Mauger	5,110,373	May 05, 1992

Huster et al. (Huster), *Sensors and Actuators*, "Vertically Structured Silicon Membranes by Electrochemical Etching," A21-A23, 1990, pages 899-903.

Claims 1 through 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wise in view of Huster or Mauger. We reverse this rejection for reasons which follow.

Pursuant to the provisions of 37 C.F.R. § 1.196(b), we make the following new rejection:

Claims 11-18 are rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Huster.

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. We make reference to the examiner's answer (Paper No. 16, mailed September 21, 1994) for the examiner's complete reasoning in support of the rejection, and to the appellants' brief (Paper No. 15, filed July 05, 1994) and reply brief (Paper No. 17, filed November 21, 1994) for the appellants' arguments thereagainst.

OPINION

Wise describes a semiconductor thermopile detector **10** comprising a thick semiconductor rim **20** containing an aperture **22** through which infrared radiation is detected by thermopiles **24** which span portions of the aperture **22** and the rim **20** (Fig. 2A). The thermopiles **24** comprise a plurality of thermocouples **32** formed of a first layer of polycrystalline silicon **34** and a metal layer **36** and are connected to output leads and processing circuitry (Fig. 2B). Aperture **22** is preferably spanned by a dielectric diaphragm **40** to support the thermopile **24**, although the thermopile **24** may be self-supporting. (Figs. 2A and 3; col. 5, lines 25-32 and 54-67). Wise forms the thermopile detector by a process comprising:

diffusing a boron (i.e., “p-type”) dopant into a monocrystalline silicon substrate **50** to form rim area **20** surrounded by first **51** and second **53** undoped regions (Fig. 4A; col. 6, lines 7-20) to a thickness (i.e., “x-y”) from 1 to 20 µm, e.g., approximately 15 µm (col. 6, lines 24-30),

forming polycrystalline silicon layer **34** either on dielectric layer **40** or, if the dielectric layer **40** is not used, spanning at least portions of both the doped area **20** and the undoped area **51** of the substrate to provide support for the device after etching, typically to a thickness (i.e., “y”) of 8000 D, i.e., 0.8 µm, (Fig. 4B; col. 6, lines 60-66), and doping the polycrystalline silicon layer with phosphorus, boron, arsenic or other common silicon dopants by diffusion or ion implantation to enhance its electrical conductivity (col. 6, line 66 - col. 7, line 5),

providing additional insulating and metal layers and electronic circuitry on top of the polycrystalline silicon layer **34** to complete a thermocouple sensing assembly (Figs. 4C-4E; col. 7, lines 6-48), and

selectively etching away undoped areas **51** and **53** of the substrate **50**, but not doped rim **20** or any of the layers formed on the front side of the sensor, e.g., with an ethylenediamine-pyrocatechol (EDP) and water etch (col. 7, lines 48-53). Controlled time etch-stop (col. 3, lines 40-46; col. 8, lines 1-16) and electrochemical etch-stop techniques (col. 3, lines 47-57; col. 8, lines 17-29) are also described as alternative etches to the above diffused boron etch-stop technique.

As noted by the examiner, Wise fails to disclose or suggest forming polysilicon layer **34** by epitaxial growth (answer, page 3). However, since Huster discloses growing an epitaxial layer of n-type silicon on a p-type wafer (silicon substrate) to fabricate diaphragms of identical and controllable thickness (page 899, col. 2, first full paragraph) and Mauger describes forming a silicon diaphragm by etching away a p-type silicon substrate beneath an n-type doped layer of desired thickness formed by epitaxy (col. 3, lines 42-60; col. 4, lines 12-20; and col. 5, lines 15-25), the examiner concludes

> [i]t would have been obvious to one of ordinary skill in the art to modify Wise et al. process with an epitaxial layer on a silicon substrate as taught by Huster et al. or Mauger because a diaphragm (flexure) with rim (boss) of desired thickness on the silicon substrate can be obtained. [Answer, page 4, last full para.]

To establish a *prima facie* case of obviousness, there must be both some suggestion or motivation to modify the reference or combine reference teachings and a reasonable expectation of success. The prior art must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

Here, there is no dispute that the individual steps of diffusion, ion implantation and epitaxy are well known, art recognized techniques for providing a doped silicon layer (see e.g., Mauger, col. 4, lines 17-20) or that Huster discloses using two diffusion steps to make thick (i.e., boss) and thin (i.e., flexure) portions of vertically structured silicon diaphragm by electrochemical etching (brief, pages 5-6). Appellants argue neither Wise, Huster and/or Mauger discloses or suggests using a first diffusion step followed by a second epitaxial growth step to make relatively thick boss and relatively thin flexure sections of a structured silicon diaphragm by chemical etching in the manner claimed, wherein the desired thickness of the boss is x, the desired thickness of the flexure is y, the first diffusion depth is x-y and the epitaxial growth depth is y (brief, pages 8-9). According to the examiner, x in Wise is equal to rim **20** (x-y) *plus* polycrystalline silicon layer **34** (y) (answer, page 8) and the issue is whether it would have been obvious to provide polycrystalline silicon layer **34** of Wise as an epitaxial growth layer so as to provide a relatively thin flexure section (answer, page 4).

However, the examiner has failed to establish on this record why a self-supporting thermopile comprised of a plurality of thermocouples would have reasonably disclosed or suggested a structured silicon diaphragm, i.e., why one of ordinary skill in the art would have reasonably expected Wise's electrically conductive polycrystalline silicon layer **34** to form a flexure section given (a) that layer **34,** along with metal layer **36,** etc. forms a thermocouple and (b) that omission of the only positively recited *diaphragm* structure in Wise, i.e., dielectric diaphragm **40**, requires polycrystalline silicon layer **34** to support the device after etching (col. 6, lines 60-65). The examiner has also failed to explain why the skilled artisan would have selected the same dopant to dope both polycrystalline silicon layer **34** and rim area **20**. Rather, the only place we find a suggestion to machine silicon to form a boss diaphragm structure having relatively thick boss sections and relatively thin flexure sections by (1) providing a substrate of a first type doped silicon, (2) deeply diffusing a second type dopant only into selected areas on a surface of the first type doped silicon where the boss sections are to be formed and only to a depth (x-y) less than the desired thickness (x) of the boss diaphragm structure, (3) growing an epitaxial layer of second type doped silicon to a desired flexure section thickness (y) over the same surface of the substrate that has been diffusion doped, and then (4) etching away the first-type doped silicon so to leave the relatively thick boss sections joined by the relatively thin flexure sections, thus forming a boss diaphragm structure of desired thickness (x) is in the appellants' specification. Thus, we find that the examiner has relied on impermissible hindsight in making his determination of obviousness. *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) ("It is impermissible to engage in hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.). Accordingly, the rejection of claims 1 through 18 under 35 U.S.C.

§ 103 as being unpatentable over Wise in view of Huster or Mauger is reversed.

NEW GROUND OF REJECTION - 37 C.F.R. § 1.196(b)

Claims 11-18 are rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Huster.

Appellants' claim 11 is in product-by-process form. Thus, the patentability of the claimed invention is determined based on the product itself, not the method of making it. *In re Thorpe,* 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985).

Instead of using an epitaxial layer n-type silicon grown on a p-type wafer to form a pn-junction to manufacture membranes of identical and controlled thickness by means of electrochemical etching, Huster uses a diffused and/or ion-implanted layer to form the pn-junction, resulting in a substantial reduction in process complexity. Using two diffusions of distinctly different penetration depths, Huster obtained a vertical membrane structure having thinner membranes (i.e., flexure sections) suspended on thicker rims (i.e., boss sections) of arbitrary shape, thereby achieving improved stability of the suspension of very thin membranes. Huster describes using "standard" integrated circuitry (IC) processing steps, e.g., boron doped silicon wafers with 11-16 ohm cm resistivity were subjected to standard integrated circuitry processing to provide pn-junctions, patterns, contacts and masking layers. Junctions of thicknesses ranging from 3 to 12 µm were formed using a standard $POCl_3$ diffusion process at 1000E C or phosphorus ion implantation for predeposition followed by a drive-in diffusion at 1100E C. The wafers were etched in 40% KOH solution at 50E C with a potential of + 1.5 V at the n+ diffusion to provide etched membranes of typically 5 and 15 µm thicknesses, respectively. (See pages 899-901 and Figs. 1-7.) As noted in the specification, an annealing step is *conventional* after high energy implantation to eliminate crystal lattice defects and to diffuse dopants to the proper depth (page 7, last para.). Appellants have not challenged the examiner's finding that "specific resistivity, annealing temperature and thickness of coating layer" are art-recognized result-effective variables subject to routine experimentation and optimization (answer, page 9). Given the equivalency of epitaxial layer and diffusion/ion-implantation layers in forming the pn-junction suggested by Huster and the use of standard IC procedures for processing, masking, etching, etc. in Huster, it reasonably appears that the vertical membrane structure having thinner membranes (i.e., flexure sections) suspended on thicker rims (i.e., boss sections) of Huster is substantially identical with the instantly claimed flexure section provided in a silicon material joined with a boss section.

Appellants have argued that variations in section thickness may or may not lead to a significant variation in the bending strength of the section, e.g., a variation of +/- 0.5 µm is insignificant in a diaphragm thickness of 17 to 20 µms but the same +/- 0.5 µm variation in a flexure section of 5 µms or less results in a change of 10% or more (brief, page 12). However, none of the claims on appeal recites any limitations as to the thickness of the boss section or the flexure section. Secondly, Huster states that after the transition from the thick rim/boss section to the thin membrane/flexure section, "the thin membrane reaches a **constant** thickness" (emphasis added, page 901, last full sentence of col. 1). Therefore, since there seems to be no substantial change in the thickness of Huster's flexure section, similar to the controlled thickness flexure section produced by appellants' epitaxial layer, it appears that Huster discloses substantially the same invention as claimed.

Where, as here, the prior art product reasonably appears to fall within the scope of that which is claimed by appellant, it is reasonable to shift the burden to the appellant to provide evidence showing that the product of the prior art does not fall within the scope of appellant's claims. *In re Fitzgerald*, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980). As stated in *In re Best*, 562 F.2d at 1255, 195 USPQ at 433-34 (CCPA 1977):

> Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product. ... Whether the rejection is based on 'inherency' under 35 U.S.C. § 102, on 'prima facie obviousness' under 35 U.S.C. § 103, jointly or alternatively, the burden of proof is the same, and its fairness is evidenced by the PTO's inability to manufacture products or to obtain and compare prior art products.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1 through 18 under 35 U.S.C. § 103 is **reversed**. However, claims 11 through 18 are rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Huster.

This decision contains a new ground of rejection pursuant to 37 C.F.R. § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53, 131, 53, 197 (Oct. 10, 1997), 1203 off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 C.F.R. § 1.196(b) also provides that the appellant, <u>WITHIN TWO MONTHS FROM THE DATE OF THE DECISION</u>, must exercise one of the two following options with respect to the new ground of rejection to avoid termination of proceeedings (§ 1.197(c)) as to the rejectged claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner ....
>
> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record ...

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED - 1.196(b)

EDWARD C. KIMLIN Administrative Patent Judge	)	
TERRY J. OWENS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
CAROL A. SPIEGEL Administrative Patent Judge	)	

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APPENDIX

1. A process for forming silicon material having a boss section and a flexure section, said boss section thicker than said flexure section, said process comprising the steps of:

providing a substrate of one type doped silicon material;

diffusing another type dopant material into said substrate so as to provide another type doped silicon material at a depth (x-y) from a surface of said one type doped silicon material, said diffusing located only in the regions of the boss section, where x is the boss section thickness and y is the flexure section thickness;

epitaxially growing a layer of said another type doped silicon on said substrate to said flexure section thickness y over the surface of said substrate; and

etching away one type doped silicon material with a one type doped silicon etchant leaving said boss section having a thickness x and said flexure section having a thickness y.

2. A method of chemical machining of silicon material to provide a boss section joined by a flexure section from a substrate of p-type doped silicon material, said boss section thicker than said flexure section, said method comprising the steps of:

diffusing n-type dopant material into said substrate so as to provide an n-type material at a depth (x-y) from a surface of the p-type material, said diffusing being provided only in the regions of the boss section, where x is the boss section thickness and y is the flexure section thickness;

epitaxially growing a layer of n-type doped silicon on said substrate to said flexure section thickness y; and

etching away p-type doped silicon material with a p-type doped silicon etchant leaving said boss section having a thickness x and said flexure section having a thickness y.

10. A method of chemical machining of silicon material with a boss section joined by a flexure section from a substrate of boron doped silicon material having a resistivity of from 4 to 6 ohms-cm, said boss section thicker than said flexure section, said method comprising the steps of:

(1) providing a mask of silicon dioxide on said substrate over said flexure section;

(2) diffusing phosphorus dopant material into said substrate so as to provide a phosphorus doped silicon material at a depth (x-y) from a surface of the substrate, said diffusing being provided only in the regions of the boss section, where x is the boss section thickness and y is the flexure section thickness, said diffusing step including the steps of:

implantation of phosphorus dopant ions in said substrate; and

annealing said substrate so as to eliminate crystal lattice defects and to at least partially diffuse said phosphorus dopant ions;

(3) epitaxially growing a layer of phosphorus doped silicon on said substrate to said flexure section thickness y over the surface of the boron doped silicon substrate and the areas of diffusion phosphorus doped silicon; and

(4) etching away boron doped silicon material with a potassium hydroxide etchant leaving said boss section having a thickness x and said flexure section having a thickness y.

11. A flexure section provided in a silicon material joined with a boss section, said boss section thicker than said flexure section, said flexure section machined from a substrate of p-type doped silicon material by the process of:

diffusing n-type dopant material into said substrate so as to provide an n-type material at a depth (x-y) from a surface of the p-type material, said diffusing being provided only in the regions of the boss section, where x is the boss section thickness and y is the flexure section thickness:

epitaxially growing a layer of n-type doped silicon on said substrate to a desired flexure section thickness y over the surface of the p-type doped silicon and the areas of diffusion of n-type silicon; and

etching away p-type doped silicon material with a p-type doped silicon etchant leaving said boss section having a thickness x and said flexure section having a thickness y.

12. A flexure section in accordance with claim 11, wherein said diffusing step comprises the steps of:

implantation of n-type dopant ions in said substrate; and

annealing said substrate so as to eliminate crystal lattice defects and to at least partially diffuse said dopant ions.

13. A flexure section in accordance with claim 12, wherein said diffusing step includes, prior to said implantation step, the step of masking said substrate so as to prevent ion implantation in those areas of said flexure section.

14. A flexure section in accordance with claim 13, wherein said substrate is boron doped silicon, wherein said masking step includes providing a mask of silicon dioxide, said ion implantation step includes the step of implanting phosphorus ions.

15. A flexure section in accordance with claim 11, wherein said growing step includes the step of epitaxially growing phosphorus doped silicon.

16. A flexure section in accordance with claim 15, wherein said growing step includes the step of epitaxially growing phosphorus doped silicon having a resistivity of between 0.6 to 1.0 ohms-cm.

17. A flexure section in accordance with claim 11, wherein said etching step includes the step of electrochemical etching said substrate with at least potassium hydroxide (KOH).

18. A flexure section in accordance with claim 14, wherein said boron doped silicon material has a resistivity of between 4-6 ohm-cm.