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THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

MAILED

APR 12 1996

Ex parte PHILIP A. BOUREKAS,
YESHAYAHU MOR and SCOTT REVAK

PAT.&T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Appeal No. 95-2815
Application 07/715,525¹

ON BRIEF

Before HAIRSTON, JERRY SMITH and BARRETT, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-4, which constitute all the claims in this application. An amendment after final rejection was filed on March 17, 1994 and was entered by the examiner. This amendment overcame a rejection of claim 4 under the second paragraph of 35 U.S.C. § 112.

¹ Application for patent filed June 14, 1991.

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The claimed invention pertains to a method and apparatus for eliminating access to an on-chip cache circuit when a microprocessor is signaled that an input is to come from a main memory.

Representative claim 1 is reproduced as follows:

1. A structure for monitoring an on-chip cache in a microprocessor, said microprocessor having a plurality of pins for accessing a main memory, comprising:

a control pin for receiving into said microprocessor a signal indicating an instruction is to be provided to said microprocessor via said pins;

a circuit receiving and responding to said indicating signal for generating a cache miss signal to prevent said microprocessor from accessing said on-chip cache for a next instruction;

a circuit receiving said cache miss signal for initiating a read access operation at said main memory to retrieve said next instruction; and

a circuit for receiving into said microprocessor an instruction provided at said plurality of pins.

The examiner relies on the following reference:

Emma et al. (Emma) 4,991,090 Feb. 05, 1991

Claims 1-4 stand rejected under 35 U.S.C. § 102(e) as anticipated by the disclosure of Emma.

Rather than repeat the arguments of appellants or the examiner, we make reference to the brief² and the answer for the respective details thereof.

² The reply brief filed December 1, 1994 was denied entry by the examiner and was not considered by us in the formulation of this decision.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that Emma does not fully meet, that is, anticipate the invention as set forth in claims 1-4. Accordingly, we reverse.

We consider first the rejection of claim 1 as anticipated by Emma. Claim 1 recites a control pin for receiving a specific signal and three circuits for performing the reception of certain recited signals and responding to such signals in a specific manner. The examiner has concluded that all of these elements are fully disclosed within Emma. Appellants argue primarily that the recited control pin and first circuit of claim 1 and their recited interrelationship are not disclosed by Emma.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 221 USPQ 385 (Fed. Cir. 1984); cert. dismissed sub nom., Hazeltine Corp. v. RCA Corp., 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). If there are any differences between the structure of the prior art and the claim, or if the structure of the claim is recited to perform operations not performed by the prior art, then a rejection under 35 U.S.C. § 102 would generally be inappropriate. All words in a claim must be considered in judging the patentability of that claim against the prior art. You cannot ignore words in a claim in evaluating patentability over the prior art. In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970).

The control pin and first recited circuit in claim 1 operate in a manner that is generally the antithesis of the way Emma or other cache control processors operate. In claim 1, when the control pin is informed that an instruction is to come directly from main memory, the on-chip cache is not used when the next instruction arrives. That is, no effort is made to attempt to

find the instruction in the cache. Ordinarily in most cache systems, the cache is always searched first before a cache miss signal is generated. In claim 1, the cache was not searched at all even though a cache miss signal is generated. In other words, the first two elements of claim 1 require that a cache miss signal be generated in response to a specific trigger signal which is unrelated to the search of the cache. Our reading of Emma is that, like most systems, Emma generates a cache miss signal only after searching the cache and finding the current instruction not present therein. Therefore, Emma does not have a circuit which responds to a specific signal received at a control pin for generating a cache miss signal as recited in claim 1. If Emma only generates a cache miss signal after searching the cache, which appears to be the case, then Emma does not meet all the specific limitations recited in claim 1.

Appellants have also pointed out that Emma does not disclose an on-chip cache as recited in claim 1. The examiner has responded that the location of the cache does not affect the scope of the invention, and to make something integral is generally not given patentable weight [answer, page 5]. While the integration

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of known components may generally be an obvious design consideration, the rejection here is on anticipation rather than obviousness. The examiner's premise that the scope of an on-chip cache is the same as an off-chip cache cannot be agreed with. The cache being on-chip is a specific limitation not met by off-chip caches.

The examiner also dismisses the recitation of the control pin because the use of pins was standard in the art [answer, page 6]. However, the fact that pins were standard in the art does not mean that the use of a pin to receive a specific signal and have a circuit perform a specific response upon receipt of that signal as set forth in claim 1 was fully disclosed by the prior art or that such a combination would necessarily have been obvious in view of such known standards. It is the manner in which known elements are combined that form the basis of the invention. The examiner has not shown that these elements as combined in the invention of claim 1 were known or suggested by the teachings of Emma.

For all the reasons discussed above, we do not sustain the rejection of claim 1. Since claim 2 depends from claim 1 and

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Edward C. Kwok
Skjerven, Morrill, MacPherson,
Franklin and Friel
25 Metro Dr.
Ste. 700
San Jose, CA 95110