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THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

MAILED

JUN 20 1996

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

PAT & TM OFFICE  
BOARD OF PATENT APPEALS  
AND INTERFERENCES

~~Ex parte~~ SATOSHI HORI, TERUYO OMORI  
and MAKOTO SAKAGAMI

Appeal No. 95-1683

Application 07/739,591

ON BRIEF

Before CALVERT, HAIRSTON and FLEMING, Administrative Patent Judges.  
FLEMING, Administrative Patent Judge.

DECISION ON APPEAL

<sup>1</sup> Application for patent filed July 24, 1991.

This is a decision on appeal from the final rejection of claims 1 through 3, all of the claims present in the application.

The invention relates to fault diagnosis devices for diagnosing causes of faults of various devices and apparatus such as industrial machines. Appellants disclose on pages 4 and 5 of the specification that Figure 1 is a block diagram showing the organization of the fault diagnosis devices. Appellants disclose that the main memory 1 stores a fault tree in which each node corresponds to a hardware sub-unit of the device under test 6. Appellants further disclose that at each node are stored test tables and probability fault tables.

On pages 6 and 7, Appellants disclose that Figure 3 shows in greater detail the organization of the fault tree and fault branch tree loaded in the main memory of the fault diagnosis device of Figure 1. As shown in Figure 3, the root node 8 has three child nodes, a gas unit node 9a, an alarm unit node 9b and a boiler unit node 9c which correspond to three sub-units of the device under test, the gas unit, the alarm unit and the boiler unit, respectively. Test tables 2, 2a, 15 are associated with each node. Figure 4 shows the details of the test table stored at the root node 8. Detection table 10 stores names

of detector units, TEMP1 and TEMP2, which detect the temperatures within the device under test. When the search/inference unit 3 selects this test table 2, the detector units that are stored in table 10 are activated and the command parameters stored in the second column of the detection table 10 are transmitted to the detector units. The detector detects the values as commanded and stores the values in the third column of the detection table 10. A judgment table 11 stores the test conditions and the search/inference unit 3 performs these tests and stores the judgment of these tests in the last column of the judgment table 11. A fault probability table 12 stores the values of fault probability and the names of the child nodes associated with the results of the judgments stored in the judgment table 11. Appellants disclose on pages 8 and 9 of the specification that if the search/inference unit 3 determines the fault probability exceeds a predetermined threshold the system proceeds to the child node for further test.

The independent claim 1 is reproduced as follows:

1. A fault diagnosis device for determining a cause of fault of a device under test, comprising:

detector means for detecting parameters of a device under test;

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memory means;

a fault tree stored in said memory means and having nodes corresponding to respective sub-units of said device under test, whereby said fault tree has a tree structure corresponding to a hardware organization of said device under test;

test tables stored in said memory and associated with respective nodes of said fault tree, each test table including: a description of at least one parameter to be detected by said detector means; at least one test condition with respect to the parameter detected by said detector means; and a fault probability table representing fault probabilities and names of child nodes corresponding to respective results of said test condition; and

search/inference means for searching and for determining a cause of fault of said device under test in accordance with said fault tree and said test tables;

wherein at least one of said nodes has at least three child nodes and the test table associated with the node having at least three child nodes includes: a description of at least two parameters to be detected by said detector means; at least two test conditions with respect to the parameters detected by said detector means; and a fault probability table representing fault probabilities and names of child nodes corresponding to respective patterns of results of said test conditions.

The Examiner relies on the following references:

Denny	4,817,092	Mar. 28, 1989
Matsumoto	4,839,823	Jun. 13, 1989
Hogan, Jr. et al. (Hogan)	4,841,456	Jun. 20, 1989
Oda et al. (Oda)	5,127,005	Jun. 30, 1992

(filed Sep. 19, 1990)

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Cantone et al. (Cantone), "IN-ATE: Fault Diagnosis as Expert System Guided Search," Automated Reasoning Corporation, New York, 1987, PP 1-47.

Claims 1 and 2 stand rejected under 35 U.S.C. § 103 as being unpatentable over Cantone, Denny, Oda and Matsumoto. Claim 3 stands rejected under 35 U.S.C. § 103 as being unpatentable over Cantone, Denny, Oda, Matsumoto and Hogan.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs<sup>2</sup> and answer for the respective details thereof.

#### OPINION

We will not sustain the rejection of claims 1 through 3 under 35 U.S.C. § 103.

The Examiner has failed to set forth a prima facie case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention

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<sup>2</sup> Appellants filed an appeal brief on March 14, 1994 which will be referenced as the brief and a reply appeal brief on June 24, 1994 which will be referenced as the reply brief.

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by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. See In re Sernaker, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." Para-Ordnance Manufacturing v. SGS Importers International, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) citing W. L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Appellants argue in the brief on page 7 that Cantone does not teach the use of fault trees having nodes corresponding to respective sub-units of a device under test, whereby the fault tree has a tree structure corresponding to a hardware organization of the device. Appellants argue that Cantone instead teaches the use of a unit under test model, having multiple test points where the nodes of the fault tree correspond to potential faults and symptoms and not to respective sub-units of the device under test.

In the answer on page 6, the Examiner states that Cantone does disclose the use of fault trees having nodes corresponding to

respective sub-units of a device under test on page 32, Figure 4.1(b). The Examiner argues that Cantone shows in Figure 4.1(b) a fault tree having nodes corresponding to the sub-units of a oscilloscope under test.

Appellants respond to this new point of argument raised in the Examiner's answer on pages 3 and 4 of the reply brief. There Appellants point to Cantone at page 31 which explains that T1 is a test point for an oscilloscope corresponding to the z-axis input to a CRT. Cantone discloses that a test is performed at test point T1 and this test can fail in one of two ways: either there is no trace on the CRT screen at all or there is a trace but it is turning on and off at inappropriate times. The causes of the "no trace" symptom may be either a bad z-axis amplifier or a bad CRT circuit. The causes of the "bad timing" symptom may be either a bad chop blanking circuit or a bad sweep unblanking circuit. Appellants argue that the nodes of the fault tree at page 32 of Cantone correspond to symptoms of a fault, and do not correspond to respective sub-units of a device under test whereby the tree structure corresponds to a hardware organization of the device under test as required by Appellants' claims. The Examiner responded in a communication mailed January 10, 1995 that the reply

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brief has been entered but no further response by the Examiner is deemed necessary.

Appellants' claim 1 recites a "fault diagnosis device for determining a cause of fault of a device under test, comprising: ... a fault tree stored in said memory means and having nodes corresponding to respective sub-units of said device under test, whereby said fault tree has a tree structure corresponding to a hardware organization of said device under test." Upon a closer inspection of Cantone, we agree with Appellants that Cantone fails to teach this claimed limitation. The nodes shown in the fault tree in Cantone's Figure 4.1(b) correspond to a test performed at point T1 that determines either there is no trace, node labeled trace, or there is bad timing, node labeled timing. Cantone simply states that if it is determined there is no trace then the fault is due to a bad z-axis amplifier, a bad CRT-circuit or a low voltage supplied to either of these. Similarly, Cantone simply states that if it is determined there is bad timing, then the fault is due to bad chop blanking or bad sweep unblanking. Thus, Cantone is teaching a binary fault tree in which a test corresponds to the root node of the fault tree and the results correspond to faulty circuits. Cantone does not teach a fault tree

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that is organized in which each node corresponds to respective sub-units of the device under test whereby the fault tree has a tree structure corresponding to a hardware organization of the device under test as required by Appellants' claims.

Appellants further argue on pages 7 and 8 of the brief that Denny does not teach test tables that are associated with respective nodes of a fault tree corresponding to particular hardware sub-units of a device under test as set forth in Appellants' claim 1. On page 4 of the answer, the Examiner argues that Denny shows in Figures 17-43(c) the use of a number of test tables. Appellants respond in the reply brief that it is true that Denny discloses test tables which identify all possible tests supported by the diagnostic cards, but does not teach test tables that are associated with respective nodes corresponding to respective sub-units of the device under test. The Examiner has not responded to this argument or supplied us with any support that Denny teaches Appellants' claimed limitation. Upon a close inspection of Denny, we fail to find that Denny teaches the use of test tables at a node that correspond to a sub-unit of the device under test for determining a cause of a fault.

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Similarly, Appellants argue on page 8 that Matsumoto fails to teach associating with nodes of a fault tree a probability table. We agree. Matsumoto does teach a probability table, but fails to teach a probability table associated with each respective node corresponding to respective sub-units under test of a fault tree representing fault probabilities and names of child nodes corresponding to respective results of the test condition as recited in Appellants' claim 1.

Furthermore, we fail to find any suggestion in the prior art to suggest to one skilled in the art to modify the cited references to obtain Appellants' claimed invention. The Federal Circuit stated that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992), citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). Therefore, we will not sustain the Examiner's rejection of Appellants' claims 1 through 3 as being unpatentable under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.



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