

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

MAILED

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

SEP 27 1996

PAT.&T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEN SAKAMURA
and
AKIRA OHTSUKA

Appeal No. 95-0510
Application 07/873,525¹

ON BRIEF

Before THOMAS, HAIRSTON and KRASS, Administrative Patent Judges.
THOMAS, Administrative Patent Judge.

¹ Application for patent filed April 21, 1992. According to appellants, the application is a continuation of Application 07/668,316, filed March 13, 1991, abandoned; which is a continuation of Application 07/171,624, filed March 22, 1988, abandoned.

Appeal No. 95-0510
Application 07/873,525

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 7, which constitute all of the claims in the application.

Representative claim 1 is reproduced below:

1. A data processor which is provided with a main memory and a cache memory storing parts of the contents of said main memory, and which executes an operating system and user programs, and executes instructions divided into at least a low priority privilege level group and a higher priority privilege level group, said data processor comprising:

means for preliminarily fetching instructions in a program from the main memory to the cache memory;

means for executing a predetermined instruction, included in a user program and being in the low priority privilege group, where the predetermined instruction always invalidates the contents of said cache memory whenever the predetermined instruction is executed so that instructions following said predetermined instruction must be fetched from said main memory when the data processor is executing said user program.

The following references are relied on by the examiner:

Papworth et al. (Papworth)	4,760,519	Jul. 26, 1988 (filed Sep. 15, 1986)
Shintani et al. (Shintani)	4,760,520	Jul. 26, 1988 (filed Oct. 31, 1985)
Nishimukai et al. (Nishimukai)	4,989,140	Jan. 29, 1991 (effective filing date Mar. 17, 1986)
Furht et al. (Furht), "A Survey of Microprocessor Architectures for Memory Management," <u>Computer</u> , vol. 20, no. 3, pages 48 to 67 (Mar. 1987)		

Appeal No. 95-0510
Application 07/873,525

Harman et al. (Harman), The Motorola MC68000 Microprocessor Family: Assembly Language, Interface Design, and System Design, pages 92, 93, 198-201, 285-301 (Prentice-Hall Inc., 1985)

Claims 1 to 7 stand rejected under 35 U.S.C. § 112, first paragraph, as being based on an original specification which lacks support for the invention as is now claimed.

Claims 1 to 7 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Nishimukai in view of Furht or Harman.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Harman in view of Papworth or Shintani.

Rather than repeat the positions of the appellants and the examiner, reference is made to the Briefs and the Answer for the respective details thereof.²

² We note that the letter from the examiner dated August 16, 1996 indicates that the Reply Brief received May 11, 1994 has been "considered" by the examiner. Our review of the record indicates that the Reply Brief was apparently entered as well. Therefore, we have considered it in our deliberations.

Appeal No. 95-0510
Application 07/873,525

OPINION

Rejection Under 35 U.S.C. § 112, First Paragraph

We turn first to the rejection of claims 1 to 7 under 35 U.S.C. § 112, first paragraph. Initially, we note that the examiner's reasoning for lack of "support" for the claimed invention of claims 1 to 7 implicitly refers to the written description requirement of 35 U.S.C. § 112, first paragraph. In re Higbee, 527 F.2d 1405, 1406, 188 USPQ 488, 489 (CCPA 1976).

The test to be applied under the written description portion of 35 U.S.C. § 112, first paragraph, is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventors had possession at that time of later claimed subject matter. Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117, reh'g. denied (Fed. Cir. July 8, 1991) and reh'g. en banc denied (Fed. Cir. July 29, 1991). It is noted that originally filed independent claims 1, 3, and 5 were amended on August 19, 1991 to include the feature that the means for executing a predetermined instruction is "included in a user program." Originally filed independent claim 6 was amended on April 21, 1992, to include the feature that the means for executing a predetermined instruction is "included in a user program," and that the means for executing

Appeal No. 95-0510
Application 07/873,525

a predetermined instruction "always" invalidates the branch history information.

The manner in which the specification as filed meets the written description requirement is not material. The requirement may be met by either an express or an implicit disclosure. In re Wertheim, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976). An invention claimed need not be described in ipsis verbis in order to satisfy the written description requirement of 35 U.S.C. § 112, first paragraph. In re Lukach, 442 F.2d 967, 969, 169 USPQ 795, 796 (CCPA 1971). The question is not whether an added word was the word used in the specification as filed, but whether there is support in the specification for the employment of the word in the claims, that is, whether the concept is present in the original disclosure. See In re Anderson, 471 F.2d 1237, 1244, 176 USPQ 331, 336 (CCPA 1973).

In the instant case, as to the newly added limitation of claims 1, 3, 5, and 6 of the purge instruction being "included in a user program," appellants argue that the description of the prior art at pages 2 to 3 of the originally filed specification and the fact that the "data processor . . . invalidates the instruction cache . . . even when executing user-programs" (emphasis in original) (Brief, pages 5 to 6 (citing specification, summary of the invention at page 4, lines 10 to 12)) would

Appeal No. 95-0510
Application 07/873,525

reasonably convey to the artisan that appellants had possession of the claimed subject matter at the time of filing.

In accordance with appellants' reasoning (Reply Brief, top of page 3), we find that the originally filed specification's differentiation between an operating system executing a purge instruction as having been known in the prior art (specification, page 3) and a user program executing a purge instruction as being the object of appellants' disclosed invention (specification, page 4) implicitly discloses and reasonably conveys to the artisan, in context, that the purge instruction was "included in a user program." This appears to be consistent with the case law cited earlier for the following reasons:

Appellants' specification specifically discusses that the drawback of the prior art was that execution of purge instructions by the operating system prevented conventional data processors from "judg[ing] whether the program is correctly executed, or not" (specification, bottom of page 3). Appellants' specification further states that the object of the disclosed invention was "to eventually ensure smooth coordination between the instruction lines of the main memory and the actually processed instructions" (specification, page 4). In order to accomplish this, and overcome the drawbacks of the conventional

Appeal No. 95-0510
Application 07/873,525

data processor program sequence as shown in figure 4, appellants implement the program execution sequence of figure 5 instead.

We note that figure 5 differs from figure 4 only in that the purge instruction (PIB) has been inserted into the sequence. Figures 4 and 5 are implicitly disclosed as "user programs" since they are executed by the data processor and by CPU 1 (see Brief, page 6). Thus, the inclusion of the purge instruction in figure 5 reasonably conveys to the artisan the concept that the purge instruction be "included in a user program." Therefore, we generally agree with appellants that the "included in a user program" language of claims 1 to 7 is supported by the originally filed specification, and therefore reverse the rejection under § 112, first paragraph.

As to the newly added limitation of claim 6 that the means for executing a predetermined instruction "always" invalidates the branch history information, appellants argue that page 6, lines 4 to 12 of the originally filed specification (stating that the "program . . . executes the PIB instruction . . . to invalidate . . . [the] branch prediction system") and page 7, lines 5 to 7 of the originally filed specification (stating that the "CPU 1 . . . executes [the] [sic] PIB instruction" in order to invalidate the cache memory) provide support thereof.

Appeal No. 95-0510
Application 07/873,525

In accordance with appellants' reasoning (Brief, pages 7 to 8), we find that figure 5 of the originally filed specification, taken in context, implicitly discloses and reasonably conveys to the artisan that the purge instruction (PIB), which invalidates the branch history information, is always part of the program sequence. Note also the abstract at page 14 of the specification as filed with respect to the invalidation of "the content or branch records." Although the originally filed specification does not state in ipsis verbis that the purge instruction "always" invalidates the branch history information, we find that in context, to the artisan, figure 5 and the noted portions of the specification as filed reasonably support the employment of the word in the claims, that is, we find that the entire disclosure supports the concept. This appears to be consistent with the case law cited earlier.

We observe that the "always . . . invalidates" language of independent claim 6 is present in independent claims 1 and 3, although not recognized by the examiner to be a problem since no § 112, first paragraph, rejection was made on this basis as to claims 1 and 3. Nonetheless, we find support for this limitation in all of the claims.

Appeal No. 95-0510
Application 07/873,525

Therefore, we generally agree with appellants that the "always" language of claims 6 and 7, as expressed by the examiner and as included in claims 1 and 3 as just discussed, is supported by the originally filed specification. Accordingly, we reverse the rejection under § 112, first paragraph.

Rejections Under § 103

After carefully studying the entire record before us, we will reverse both the § 103 rejection of claims 1-7 over Nishimukai in view of Furht or Harman, and the § 103 rejection of claims 6 and 7 over Harman in view of Papworth or Shintani.

Rejection Under § 103: Over Nishimukai in view of Furht or Harman

As to the first § 103 rejection, of claims 1 to 7, we generally agree with appellants' arguments in the Brief and Reply Brief that Nishimukai teaches a "specific" purge instruction for invalidating a cache memory in a data processor, and that Furht or Harman teaches a data processor having a supervisory mode having high priority and a user mode having lower priority. We also agree with appellants' arguments that the "user program" in Nishimukai controls several "general" or "basic" instructions which are processed through the FIFO memory 34 and the decoder 35, and that the "operations system" controls the "specific" or

Appeal No. 95-0510
Application 07/873,525

"excepted" functions such as a "predetermined instruction to invalidate" contents of the cache memory (a purge instruction, or PIB). See figure 4:

The weight of the evidence does not support the examiner's position that "the insertion of a known instruction into a user program should not be patentable" (Answer, page 10). Indeed, we observe that appellants consider the placement of the purge function into a user program (see figure 5) to be the inventive step which is the crux of the disclosed invention. See appellants' specification, pages 6 to 7.

Thus, a key issue in the rejection of claims 1-7 under § 103 is the examiner's reliance on Harman (at page 198, et seq.) to teach or suggest that "a conditional branch can be executed in the user mode" (Answer, page 6). We find that Harman would not have reasonably taught or suggested to the artisan the recited feature of claims 1 to 7 of "executing a predetermined instruction, included in a user program and being in [a] low priority privilege group" for purposes of invalidation of a cache memory (claims 1 to 5) or a branch prediction mechanism (claims 6 and 7). We find no teaching or suggestion at page 198 of Harman, and can only speculate, that the conditional branch instruction is executed "in a user program." Furthermore, we agree with

Appeal No. 95-0510
Application 07/873,525

appellants that Harman suggests teaching away from such a feature, since "[t]he occurrence of any exception [such as privileged instructions] causes the appropriate routine to execute in the supervisor mode" (Harman, page 92). As discussed by appellants in their disclosure, it is conventional that purging or privileged instructions be executed by the operating system (appellants' specification, page 3). Thus, it appears that these would be "exceptions" which would have been processed by Harman's supervisory mode (an operating system), and not by a user mode (user program).

We find that the deficiencies of Harman are not overcome by Nishimukai. We generally agree with appellants' position (response of January 30, 1992, pages 2 to 3; amendment of April 21, 1992, pages 7 to 8) that the basic, or general, instructions and the purge instruction are separate instructions which are processed differently by the data processor. See Nishimukai's figure 4. We find that Nishimukai's purge instruction is generated either by the main memory 5 (see column 4, lines 41 to 43) or the address transformation device, which is either inside the chip or "outside" of the processor (see column 4, lines 59 to 61; and column 5, lines 1 to 18). Again, we find no teaching or suggestion in Nishimukai, and can only speculate, that the purge instruction is executed "in a user program."

Appeal No. 95-0510
Application 07/873,525

The examiner states in both the final rejection and the Answer that Nishimukai (column 4, lines 41 to 43) teaches that "the purge instruction is read out from memory along with the basic instructions" (final rejection, page 4; Answer, page 7), and that in the alternative, such a feature would have been obvious (see final rejection, pages 4 to 5; Answer, pages 7 to 8). We think the examiner's reliance on column 4, lines 41 to 43 is misplaced, since these lines refer to the main memory 5 and not the FIFO memory 34 (which processes general/basic instructions which are conventionally executed by a user program). We also find that such a feature would not have been obvious, even in light of the combined teachings of the references.

Although appellants admit that "operation modes (privileged mode/user mode) in a processor are well known by Furht and Harman," and appellants "recognize[] that the existence of these modes is common in the prior art" (Reply Brief, pages 5 to 6), we cannot agree with the examiner that this in any way would have made it obvious to insert a predetermined or purge instruction into a user program in the lower priority or user mode.

We agree with appellants that the existence of the low priority and high priority modes is not dispositive to the issues in this case. Nishimukai teaches a processor having a cache

Appeal No. 95-0510
Application 07/873,525

memory which executes a "predetermined instruction" (purge instruction). Appellants admit that, Furht or Harman teaches privilege and user modes in a processor (the MC 68000). As discussed earlier, we find the examiner's reasoning for the combination to be speculative. For us to sustain the examiner's rejection we would have to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejection under 35 U.S.C. § 103. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057, reh'g denied, 390 U.S. 1000 (1968). Therefore, we find that the applied references, when taken as a whole, would not have taught or suggested the recited data processor of claims 1 to 7.

Accordingly, we find that the applied references, taken singly or in any combination thereof, would not have taught or suggested the recited invention of claims 1 to 7.

Rejection Under § 103 Over Harman in view of Papworth or Shintani

As to the second rejection under § 103, of claims 6 and 7, we generally agree with appellants' arguments in the Brief and Reply Brief that "the Examiner has pointed out no reference which teaches directly or inherently suggests including a predetermined instruction in a user program at the low priority level group to always invalidate the branch history information upon execution" as claimed (Brief, page 10).

Appeal No. 95-0510
Application 07/873,525

Specifically, we find that Harman fails to teach or suggest a predetermined or purge instruction "included in a user program" as just discussed earlier with respect to the first § 103 rejection. Although we agree with the examiner, and appellants also admit, that Papworth or Shintani discloses the feature of purging (flushing, invalidating, or clearing), we cannot agree that either reference would have fairly taught or suggested to the artisan the inclusion of such an instruction "in a user program."

Here, as with the first § 103 rejection discussed earlier, for us to sustain the examiner's rejection we would have to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejection under 35 U.S.C. § 103. Warner, 379 F.2d at 1017, 154 USPQ at 178. Therefore, we find that the applied references, when taken as a whole, would not have taught or suggested the recited data processor of claims 6 and 7.

DECISION

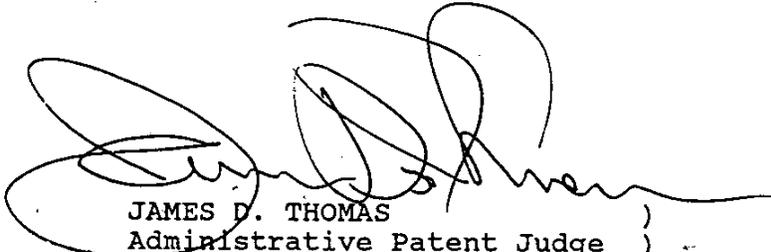
In view of the foregoing, the decision of the examiner rejecting claims 1 to 7 under 35 U.S.C. § 112, first paragraph, is reversed.

Appeal No. 95-0510
Application 07/873,525

The decision of the examiner rejecting claims 1 to 7 under 35 U.S.C. § 103 over Nishimukai in view of Furht or Harman is also reversed.

Lastly, the decision of the examiner rejecting claims 6 and 7 under 35 U.S.C. § 103 over Harman in view of Papworth or Shintani is reversed.

REVERSED



JAMES D. THOMAS
Administrative Patent Judge)



ERROL A. KRASS
Administrative Patent Judge)

) BOARD OF PATENT
) APPEALS AND
) INTERFERENCES

HAIRSTON, dissenting

I respectfully dissent from the opinion of the majority. I have carefully considered the entire record and I would affirm the 35 U.S.C. § 112 rejection, first paragraph, of claims 1 through 7. I would reverse the 35 U.S.C. § 103 rejection of claims 1 through 7. Additionally, I would reject

Appeal No. 95-0510
Application 07/873,525

claims 1 through 7 under 35 U.S.C. § 112, second paragraph, under the provisions of 37 CFR § 1.196(b).

The majority finds that the phrase provided within the "SUMMARY OF THE INVENTION" (specification, page 4) stating that "[t]he data processor related to the invention invalidates the instruction cache and the instruction pipeline even when executing user-programs" provides sufficient support for the claimed instruction being included in a user program (emphasis added) (Decision, page 5). I respectfully disagree. There is nothing within this portion of the specification to suggest that, at the time of filing the application, appellants had within their possession the concept of including the purge instruction in a user program. As stated by the examiner, there is nothing to suggest that "because the PIB instruction is executed by the CPU that it is part of the user program" (emphasis added) (Answer, page 9). The specification states that the purge instruction may be executed "even when executing user programs," not that the purge instruction is included within a user program.

The majority states that the specification differentiates between an operating system executing a purge instruction of the prior art and "a user program executing a purge instruction" of the invention, and thus "implicitly discloses and reasonably

conveys to the artisan . . . that the purge instruction was 'included in a user program'" (Decision, page 6). I do not find within the language of the specification the statement, "a user program executing a purge instruction." Again, the specification simply states that "[t]he data processor related to the invention invalidates the instruction cache and the instruction pipeline even when executing user-programs" (emphasis added) (specification, page 4). From the use of the word "when," a skilled artisan could reasonably interpret the statement to mean that the operating system is executing the purge instruction, while (when) the user programs are also being executed. Alternatively, a skilled artisan could reasonably interpret the statement to mean that the user program executes the purge instruction, as is the position of the majority. But given this ambiguity, I cannot state with certainty that appellants possessed the invention, as is now claimed, at the time of filing the instant application.

First, the majority interprets the specification to find that the disclosure teaches "a user program executing a purge instruction" (emphasis in original) (Decision, page 6). As indicated supra, there is no express statement within the specification that a user program executes the purge instruction. Second, the majority expounds on that interpretation of the

Appeal No. 95-0510
Application 07/873,525

specification to find, from it, that the specification "implicitly discloses and reasonably conveys to the artisan that the purge instruction was 'included in a user program'" (Decision, page 6). It was necessary for the majority to undertake two interpretative steps to derive the claimed purge instruction being "included in a user program" from the disclosed purging being performed "even when executing user programs." I do not agree with such multiple interpretations of a phrase of the specification to arrive at a finding of support within the specification sufficient to satisfy the written description requirement.

The majority finds that the specification identifies a drawback of the prior art as being the result of purge instructions executed by the operating system in conventional data processors (Decision, page 6). I find no such assertion explicitly mentioned within the specification. As stated by the majority (Decision, page 6), the object of the invention was to ensure coordination between instruction lines of the main memory and those instructions actually processed. The specification does not provide a comparison of the purge instruction being included in the user program as opposed to the operating system, as the majority asserts. The majority also states (Decision, page 7) that "Figures 4 and 5 are implicitly disclosed as 'user

Appeal No. 95-0510
Application 07/873,525

programs'" relying on the arguments of the appellants in support of their position. I find neither explicit nor implicit support for this position within the specification.

Accordingly, I find that the examiner's rejection was warranted, and I would affirm the 35 U.S.C. § 112, first paragraph, rejection of claims 1 through 7, with regard to the claimed instruction means being included in a user program.

The examiner rejected claims 6 and 7 (Answer, page 4) finding no support within the specification for the claim language requiring the purge instruction "to always invalidate the branch history information." Neither the originally filed claims nor the cited portions of the specification specifically mention the claimed "branch history information," nor do they provide a suggestion that the purge instruction will always invalidate the branch history information.³ The majority relies on Figure 5 of the specification to find an implicit disclosure of the purge instruction always invalidating the branch history information (Decision, page 6). I respectfully disagree, finding no such

³ It is important to note that claims 1 and 3 also include a requirement that the instructions will "always" invalidate the stored instructions, but those claims specify that the invalidation occurs only when the purge instruction is executed.

Appeal No. 95-0510
Application 07/873,525

always invalidating requirement from the flow chart of Figure 5. Accordingly, I find that the examiner properly rejected these claims as failing to provide support for the invention as is now claimed. Therefore, I would affirm the 35 U.S.C. § 112, first paragraph, rejection of claims 6 and 7, with regard to the claimed instruction always invalidating the branch history information.

Turning to the prior art rejection, I find that considerable speculation as to the meaning of the terms employed and assumptions as to the scope of the claims would be required to provide a basis for a rejection under 35 U.S.C. § 103, particularly in light of the fact that there is nothing in the specification to support these terms, and especially given the confusion these newly added terms have created. Accordingly, such a rejection should not be made.⁴ In re Steele, 305 F.2d 859, 862, 134 USPQ 292, 295 (CCPA 1962).

In view of the foregoing, I would institute a new indefiniteness rejection under the provisions of 37 CFR

⁴ As correctly indicated by appellants (Reply, page 2), issues concerning obviousness of the claimed invention should not be reached if the written description issues are not overcome.

Appeal No. 95-0510
Application 07/873,525

§ 1.196(b) that corresponds to the rejection under 35 U.S.C.
§ 112, first paragraph.


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Appeal No. 95-0510
Application 07/873,525

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