

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

MAILED

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MITCHELL A. STONES and JEFFREY M. MICHELSEN

Appeal No. 94-2869
Application 07/661,739¹

ON BRIEF

Before HAIRSTON, KRASS and FLEMING, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 14 through 20, constituting all the claims pending in the application.

The invention is directed to a programmable DRAM interface controller which permits programming the row address strobe (RAS) and the column address strobe (CAS) access timing

¹ Application for patent filed February 27, 1991.

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signals in units of one-half the microprocessor clock cycle so as to reduce access timing from $N + 1$ microprocessor wait states to an average of $N + \text{one-half}$ microprocessor wait states by repetitively varying the access timing from $N + 1$ to N wait states. This results in enhanced operating efficiency of the computer.

Independent claim 14 is reproduced as follows:

14. For use in an $N + 1$ wait state computer system having a microprocessor for controlling memory cycle start signal, bank select signal and same page access signal and having operatively associated therewith a bus cycle controller having RAMSET, RASTMA, RASTMB, CASTMA and CASTMB registers; a system clock for generating microprocessor clock cycles; and, a plurality of DRAM memory devices operable at an average of $N + \text{one-half}$ microprocessor wait states, said DRAM memory devices being responsive to DRAM RAS and DRAM CAS access timing signals generated by a DRAM controller operatively associated with said microprocessor and said DRAM memory devices; an improved programmable DRAM controller comprising: means to program said DRAM RAS and DRAM CAS access timing signals in units of one-half said microprocessor clock cycle to reduce said DRAM RAS and said DRAM CAS access timing from $N + 1$ microprocessor wait states to an average of $N + \text{one-half}$ microprocessor wait states by repetitively varying said access timing from $N + 1$ to N wait states.

The examiner relies on the following references:

Amitai	4,797,850	Jan. 10, 1989
Rubinstein	5,077,686	Dec. 31, 1991

Claims 14 through 20 stand rejected under 35 U.S.C. 103 as unpatentable over Amitai in view of Rubinstein.

Rather than reiterate the arguments of appellants and the examiner, reference is made to the brief and answer for the respective details thereof.

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OPINION

In determining the issue of obviousness we look to the collective teachings of the references relied upon by the examiner and to whether the hypothetical person of ordinary skill in the art, familiar with such teachings, would have found it obvious to make a structure corresponding to what is claimed. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983). It is incumbent upon the examiner to provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

The examiner applies Amitai for the basic teaching of a DRAM controller with multiple column address and row address strobe signals, i.e., Amitai teaches essentially what appellants disclose as prior art in the background section of their specification. The examiner then applies Rubinstein as a motivation for the skilled artisan for changing the access timing in a system such as Amitai's. The examiner's rationale is that Rubinstein's teaching of dividing the 32 Mhz clocking frequency by 2 in order to provide a 16 Mhz frequency, citing column 4, lines 22-46 of Rubinstein, is "equivalent" to the enablement of

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RAS and CAS signals every $N + \text{one-half}$ microprocessor wait states [answer, page 3].

The examiner has failed to present a prima facie case of obviousness.

Claim 14 specifically recites that the DRAM controller is programmed so that the RAS and CAS access timing signals are in units of one-half the microprocessor clock cycle "to reduce...access timing from $N + 1$ microprocessor wait states to an average of $N + \text{one-half}$ microprocessor wait states by repetitively varying said access timing from $N + 1$ to N wait states." We find no teaching or suggestion of this claim limitation in either of Amitai or Rubinstein or a combination thereof, agreeing with appellants [at page 13 of the brief] that the applied references do not "teach or even suggest that differing cycles with differing wait states can be repetitively combined to form a non-uniform repetitive set of operating cycles." The instant claimed invention eliminates one wait state per two access cycles. Notwithstanding the examiner's position to the contrary, this is simply not seen to be accomplished by Rubinstein's doubling or halving the clocking frequency through his "DIVIDE BY 2" circuits.

The examiner states that Rubinstein is not limited to integer frequency values [page 5 of the answer]: However, the only examples given in Rubinstein relate to integer frequency

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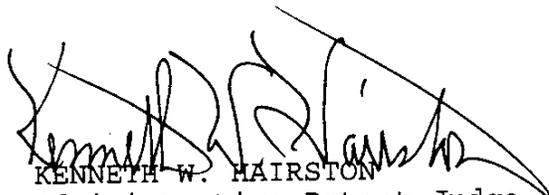
values and the examiner points to nothing indicating that Rubinstein contemplates anything other than integer values.

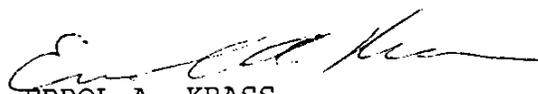
Our review of Rubinstein indicates nothing more than a clock frequency multiplication circuit wherein a clock signal of a first frequency X is multiplied by a multiple N to produce a signal of frequency NX . This permits a computer processor to operate at a higher clock speed without modification of the system clock speed. In our view, the examiner has not presented a cogent rationale for why such a teaching may be interpreted to suggest programming of DRAM RAS and CAS access timing signals from $N + 1$ microprocessor wait states to an average of $N + \text{one-half}$ microprocessor wait states by repetitively varying said access timing from $N + 1$ to N wait states, as claimed.

Since the examiner has failed to present a prima facie case of obviousness, the examiner's decision rejecting claims 14 through 20 under 35 U.S.C. 103 is reversed.

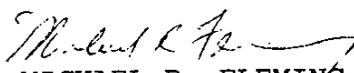
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REVERSED


KENNETH W. HAIRSTON)
Administrative Patent Judge)


ERROL A. KRASS)
Administrative Patent Judge)

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MICHAEL R. FLEMING)
Administrative Patent Judge)

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