

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MOHAMED ARAFA and SCOTT THOMPSON

Appeal No. 2004-0550
Application No. 09/802,201

ON BRIEF

Before GARRIS, WARREN and WALTZ, **Administrative Patent Judges**.
WALTZ, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's final rejection of claims 1 through 3 and 6 through 20, which are the only claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellants, the invention is directed to a decoupling capacitor¹ and its method of manufacture, where the

¹Claims directed to the capacitor device are found in the parent application no. 09/476,417, on appeal as Appeal No. 2004-0629.

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capacitor is formed on a n-type silicon region of a single crystalline silicon substrate, with a gate dielectric formed on the n-type region, a control gate formed on the gate dielectric layer, n+ type source and drain regions formed along laterally opposite sidewalls of the control gate, shallow n-type tip implants located adjacent to the source and drain regions, whereby the capacitor uses an electron accumulation layer beyond one side of the gate dielectric as one surface of the capacitor and a p-type polysilicon gate on the opposite side of the oxide layer as the other capacitor electrode (Brief, pages 3-4). Appellants assert that because of the positive bias on the p-type gate, this capacitor can provide more capacitance and does not suffer from extra polysilicon depletion as in existing devices (Brief, page 4).

Appellants state that the claims stand or fall together, with claim 1 as representative of the entire group (Brief, page 5). Accordingly, we select claim 1 from the group of claims and decide the grounds of rejection in this appeal on the basis of this claim alone. See 37 CFR § 1.192(c)(7)(2000) and *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465

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(Fed. Cir. 2002). We limit our discussion to claim 1 on appeal and to any other claims to the extent they have been separately argued by appellants. Representative independent claim 1 is reproduced below:

1. A method of forming a capacitor on a substrate having circuitry comprising:

forming a pair of shallow n-type tip implants in an n-type silicon region;

forming an n-type drain region in said n-type silicon region;

forming an n-type source region in said n-type silicon region;

forming a dielectric layer on said n-type silicon region;

forming a p+ type polysilicon gate on said dielectric layer, wherein said polysilicon gate is doped p+ type rather than n-type of said n-type drain and source regions; and

configuring said capacitor as a supply decoupling capacitor to sink and source current by coupling said polysilicon gate to a positive supply rail and by coupling said source and drain regions to a ground potential.

The examiner relies upon the following references as evidence of obviousness:

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Appel	5,605,861	Feb. 25, 1997
Rajkanan et al. (Rajkanan)	5,750,426	May 12, 1998
Dennen	5,814,869	Sep. 29, 1998
Lee et al. (Lee)	6,103,582	Aug. 15, 2000
		(filed Aug. 13, 1998)
Boden, Jr. et al. (Boden)	6,165,821	Dec. 26, 2000
		(filed Feb. 09, 1998)
Wu et al. (Wu)	6,232,208	May 15, 2001
		(filed Nov. 06, 1998)
Draper	6,285,052	Sep. 04, 2001
		(filed Sep. 26, 1997)

The following rejections are before us for review in this appeal:

(1) claims 1-3 and 6-7 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Rajkanan in view of Lee and Draper (Answer, page 4);

(2) claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Rajkanan in view of Lee, Wu and Boden (Answer, page 6);

(3) claims 10-13 stand rejected under section 103(a) over the references as in rejection (2) further in view of Draper (Answer, page 7);

(4) claims 14 and 15 stand rejected under section 103(a) over Rajkanan in view of Dennen, Appel and Draper (Answer, page 8);

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(5) claims 16-19 stand rejected under section 103(a) over the references as in rejection (1) further in view of Wu (Answer, page 10); and

(6) claim 20 stands rejected under section 103(a) over the references as in rejection (1) further in view of Boden (*id.*).

We *affirm* all of the examiner's rejections on appeal essentially for the reasons stated in the Answer and the reasons set forth below.

OPINION

The examiner finds that Rajkanan discloses a method of forming a capacitor 100" on a substrate 102, including the formation of a pair of shallow n-type tip implants in an n-type silicon region, an n-type drain region 112-2 and an n-type source region 112-1 in an n-type silicon region 104-1, a dielectric layer 108 formed on said n-type silicon region, and a polysilicon gate 110-1 formed on said dielectric layer (Answer, pages 4-5, citing Figures 4a-6). The examiner finds that Rajkanan is silent as to whether the polysilicon gate is doped p- or n-type (Answer, page 5).

The examiner finds that Lee teaches forming a polysilicon gate with p+ polysilicon material, where the polysilicon gate is

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doped p+ type rather than the n-type of the source and drain regions (Answer, page 5, citing Figure 1 and col. 2, ll. 33-49). The examiner applies Draper for the teaching to configure the capacitor as a supply decoupling capacitor by coupling a polysilicon gate 106 to a positive supply rail 114 and coupling source and drain regions 112 to a ground potential 116 (Answer, page 5). From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in this art to use the p+ type polysilicon gate of Lee in the method of Rajkanan "in order to make measurements of the characteristics of the gate oxide as taught by Lee in column 2, lines 35-37." *Id.* The examiner also concludes that it would have been obvious to use the couplings taught by Draper in the method of Rajkanan and Lee "in order to increase the net carrier concentration in the device region beneath the polysilicon gate as stated in column 4, lines 53-58 of Draper." *Id.* We agree.

Appellants agree with the examiner that Rajkanan provides no teaching or suggestion of forming a p+ type polysilicon gate on the dielectric layer, where the source and drain regions are doped n-type (Brief, page 6). Appellants argue that Lee does not

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remove the shortcomings of Rajkanan since Lee discloses the use of p+ polysilicon gate MOS capacitors for the purpose of making basic measurements of the characteristics of the gate oxide but is silent as to whether the source/drain regions are intended as p-type or n-type (Brief, page 6).

Appellants' argument is not persuasive. The examiner finds that Lee discloses that the p+ polysilicon gate MOS capacitors were formed in the n-well region (col. 2, ll. 36-38), thus suggesting to one of ordinary skill in this art that the Lee capacitor would have n-type source/drain regions (Answer, page 13). The examiner submits that the teachings of Rajkanan further support this suggestion by teaching that MOS capacitors 100" formed in a n-well 104-1 have n-type source/drain regions 112-1 and 112-2 (*id.*). In light of these uncontested findings, we agree with the examiner that Lee would have suggested a p+ type polysilicon gate MOS capacitor with oppositely doped n-type source/drain regions to one of ordinary skill in this art.

Appellants argue that Draper is "teaching away" from the claimed invention since Draper discloses a p-type gate in conjunction with a p-type source/drain and an n-type gate in

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conjunction with an n-type source/drain (Brief, pages 6-7). This argument is not persuasive for reasons stated by the examiner (Answer, pages 13-14), namely that Draper is only relied upon for the teaching of forming a supply decoupling capacitor by connecting the gate to a positive supply rail and the source/drain regions to a ground potential.

Appellants argue that n-type and p-type materials behave differently and these types of materials cannot be directly substituted to obtain the present invention (Brief, page 7). This argument is not persuasive since, as noted by the examiner (Answer, page 14), the p+ type polysilicon gate of Lee is used in place of the polysilicon gate of Rajkanan, where Rajkanan is silent as to the doping of the gate material. Therefore, contrary to appellants' argument, a p+ type material is not substituted for an n-type material.

Appellants argue that there is no motivation to combine the source/drain regions of Rajkanan with the p-type polysilicon gate for a transistor from Lee since transistors and capacitors perform entirely different functions and operate in an entirely different manner (Brief, page 7). This argument is not well

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taken since the examiner has not proposed a combination of the capacitor of Rajkanan and the transistor of Lee. The examiner's rejection relies on the combination of a p+ type polysilicon gate used for a MOS capacitor in Lee with an unspecified polysilicon gate of the MOS capacitor in Rajkanan (Answer, page 15). See Lee, col. 2, ll. 32-40. It is noted that appellants' previous arguments recognized that "Lee discloses the use of P+polysilicon gate MOS capacitors ... (see e.g., col. 2, lines 35-41)." Brief, page 6.

We note that appellants stated that the claims stand or fall together with claim 1 as representative of all the claims on appeal (Brief, page 5). However, appellants have presented arguments concerning the rejections of other claims in view of Rajkanan, Lee and other secondary references (Brief, pages 8-17). Therefore, to the extent other claims have been argued, we address these arguments below.

Appellants argue that the arsenic dosage levels taught by Wu are different than those recited in claim 8 on appeal (Brief, page 9). Appellants further argue that the teachings of Wu are in the context of transistors, not capacitors as now claimed (*id.*).

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Appellants' arguments are not persuasive for reasons stated by the examiner (Answer, pages 16-17). The examiner finds that Wu teaches dosage levels for arsenic that overlap the ranges recited in claim 8 on appeal (Answer, pages 7 and 16). Furthermore, the examiner has advanced sound reasoning as to why the implantation step of Wu for a transistor would have been applicable for doping levels in the capacitor of Rajkanan (Answer, page 17).

Appellants argue that Boden discloses a p-type polysilicon gate for use in conjunction with p+ type source/drain regions (Brief, pages 9-10). Although this argument is correct, the examiner has only applied Boden to establish the conventional doping level for p+ type polysilicon gates (Answer, page 18).

Appellants argue that there is no motivation to substitute different elements from different types of structures having dissimilar profiles and characteristics (Brief, page 10). This argument is not well taken for reasons discussed previously, namely that Lee is directed to a capacitor, not only a transistor, and the teachings of Wu directed to transistors, are also applicable to the method of Rajkanan in the formation of capacitors *and* transistors (Answer, pages 17-18).

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With regard to the rejection of claims 10-13, appellants present the same arguments discussed above with respect to Draper and the combination of Rajkanan, Lee, Wu and Boden (Brief, pages 11-12). Accordingly, we adopt our remarks from above.

With regard to the rejection of claims 14 and 15, appellants argue that Dennen is directed to transistors, and is "teaching away" from the claimed invention by teaching towards the reduction in capacitance in the device (Brief, page 13). Appellants further argue that Appel is directed to doping the gate with p-type dopants while the source/drain regions are also doped p-type, and there is no motivation for combining elements from different structures to achieve the claimed invention (Brief, page 14). These arguments are not persuasive for reasons stated by the examiner (Answer, pages 21-23), namely that Dennen does teach *some* capacitance, even if it might be "reduced." Therefore, Dennen does not teach away from a capacitor device but teaches a device with capacitance. ***See In re Gurley***, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994). The examiner also reiterates that Appel was not applied to show the claimed doping of the polysilicon gate with p-type dopants over n-type

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source/drain regions but was applied for the teaching of doping a polysilicon gate over a p-type silicon region with n-type dopants (Answer, page 22). The examiner also notes that the motivation to combine has been previously stated and appellants have not contested any specific motivation (Answer, paragraph bridging pages 22-23).

With regard to the rejections of claims 16-19 and claim 20, appellants argue that there is no motivation to combine the references as suggested by the examiner, and that it is not obvious to combine a p-type gate with a dissimilar n-type source/drain region given that the references disclose the use of a specific gate with a similarly typed source and drain (Brief, pages 15-17). These arguments are not well taken for reasons noted above, as the examiner has specifically identified motivations to combine the references (e.g., see the Answer, page 5), as well as shown that Lee teaches use of a p+ polysilicon gate with n-type source/drain regions.

For the foregoing reasons and those stated in the Answer, we determine that the examiner has established a *prima facie* case of obviousness in view of the reference evidence. Based on the

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totality of the record, including due consideration of appellants' arguments, we determine that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of section 103(a). Accordingly, we affirm all of the examiner's rejections under section 103(a) on appeal.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

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Administrative Patent Judge)	
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CHARLES F. WARREN)	APPEALS AND
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