

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex Parte HIROAKI TAKASU

Appeal No. 2003-2176
Application No. 09/778,460

ON BRIEF

Before, DELMENDO, JEFFREY T. SMITH and POTEATE, *Administrative Patent Judges*.

JEFFREY T. SMITH, *Administrative Patent Judge*.

Decision on appeal under 35 U.S.C. § 134

Applicant appeals the decision of the Primary Examiner rejecting claims 2 to 10, all of the pending claims in the application. We have jurisdiction under 35 U.S.C. § 134.¹

¹ In rendering our decision we have considered Appellant's position present in the Brief, filed February, 4, 2003 and the Reply Brief, filed June 12, 2003.

THE INVENTION

Appellant's claimed invention is directed to a method of manufacturing a semiconductor device. Representative semiconductor devices include voltage regulators and voltage detectors. (Specification, p. 5). Claims 4 and 7 are illustrative:

4. A method of manufacturing a semiconductor device, comprising the steps of:
forming an NMOS transistor having source and drain regions on a semiconductor substrate;
forming a PMOS transistor having source and drain regions on the semiconductor substrate; and
combining together an N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region to form a semiconductor thin film resistor unit;
wherein the low resistance region of the N-type thin film resistor of the semiconductor thin film resistor unit is formed simultaneously with the source and drain regions of the NMOS transistor; and
wherein the low resistance region of the P-type thin film resistor of the semiconductor thin film resistor unit is formed simultaneously with the source and drain regions of the PMOS transistor.

7. A method of manufacturing a semiconductor device, comprising the steps of:
forming an NMOS transistor having source and drain regions on a semiconductor substrate;
forming a PMOS transistor having source and drain regions on the semiconductor substrate; and
forming on the semiconductor substrate a bleeder resistance circuit having a plurality of semiconductor thin film resistor units each formed by combining together an N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region.

CITED PRIOR ART

As evidence of unpatentability, the Examiner relies on the following references:

Erdeljac et al. (Erdeljac)	5,489,547	Feb. 06, 1996
Inaba	5,877,536	Mar. 02, 1999
Kim	6,246,084	Jun. 12, 2001

THE REJECTIONS

The Examiner rejected claims 2 and 4 to 9 under 35 U.S.C. § 103(a) as being unpatentable over the combined teachings of Erdeljac and Inaba; and claims 2, 3, 7 and 10 under 35 U.S.C. § 103(a) as being unpatentable over the combined teachings of Erdeljac, Inaba and Kim. (Answer, pp. 3-4).

Appellant has indicated (Brief, page 5) that, for the purposes of this appeal, claims 2 to 6 stand or fall together and claims 7 to 10 stand or fall together. Appellant's grouping of the claims does not comply with 37 CFR § 1.192 (c)(7)(2001).² Therefore, for each ground of rejection, we will select a claim as representative of the rejected subject matter and limit our consideration thereto. *See In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir.

² Appellant's proposed groups are not exclusive. The claims 7, 8 and 9 are not subject to the same rejections.

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2002) (“If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim.”).

DISCUSSION

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by both the Examiner and Appellant in support of their respective positions. This review leads us to conclude that the Examiner’s rejections are well founded. Our reasons for this determination follow.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellant concerning the above-noted rejections, we refer to the Answer and the Briefs.

The Examiner rejected claims 2 and 4 to 9 under 35 U.S.C. § 103(a) as being unpatentable over the combined teachings of Erdeljac and Inaba; and claims 2, 3, 7 and 10 under 35 U.S.C. § 103(a) as being unpatentable over the combined teachings of Erdeljac, Inaba and Kim. We select claims 4 and 7 as representative of the rejected subject matter.

The subject matter of claim 4 is directed to a method of manufacturing a semiconductor device, comprising the combining together of an N-type thin film

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resistor having a low resistance region and a P-type thin film resistor having a low resistance region to form a semiconductor thin film resistor unit.

The subject matter of claim 7 is directed to a method of manufacturing a semiconductor device, comprising a bleeder resistance circuit. A bleeder resistance circuit is described as a plurality of semiconductor thin film resistor units each formed by combining together an N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region.

Erdeljac teaches the formation of a semiconductor device. According to the Examiner, Erdeljac teaches a process for simultaneously forming the source and drain regions of the NMOS transistor and the low resistance region of an N-type thin film. Erdeljac also teaches simultaneously forming the source and drain regions of the PMOS transistor and the low resistance region of a P-type thin film resistor. According to the Examiner, Erdeljac does not teach connecting the transistors together as a unit. (Answer, pp. 3-4). However, Erdeljac teaches that the pairing of resistors is generally known. (Col. 3, ll. 35 to 55).

According to the Examiner, Inaba teaches the connecting of resistors together to obtain a reliable dividing voltage. (Answer, p. 4). The Examiner also determined that Inaba discloses multiple resistors can be connected in series and parallel to work as one unit. (Answer, p. 5). Inaba discloses a level shifter as a

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device which shifts or reduces a source voltage and produces a level shifted voltage. (Col. 1, ll. 5-8). Inaba discloses that conventional level shifters have a voltage dividing circuit of two resistors which are connected together in series to form integrated-circuit-circuit resistors. (Col.1, ll. 33-37). The integrated-circuit-circuit resistors are described as having peculiar temperature characteristics in relation to the predetermined temperature characteristics. (Col.1, ll. 38-39).

According to the Examiner, Kim teaches the formation of resistors at the same time as the top (or bottom) electrode of the capacitor and the gate electrode. (Answer, p. 4).

The Examiner concluded that the subject matter of claim 4 was not patentable because it would have been obvious to a person of ordinary skill in the art to have connected together NMOS resistor and PMOS resistor to obtain a thin film resistor unit that has reliable dividing voltage ratio. (Answer, p. 4).

The Examiner also concluded that the subject matter of claim 7 was not patentable over the combined teachings of Erdeljac, Inaba and optionally Kim. The Examiner has determined that Inaba discloses multiple resistors can be connected in series and parallel to work as one unit. Thus, it would have been obvious to a person of ordinary skill in the art, given the combined teachings of Erdeljac, Inaba and optionally Kim, to have performed the method of manufacturing a

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semiconductor device, comprising a bleeder resistance circuit as described by claim 7.

The Appellant has not presented arguments directed to the Examiner's motivation for combining the teachings of the cited references. According to Appellant, "Inaba discloses a method of connecting resistors together in series or in parallel in a level shifter. However, contrary to the Examiner's contention, Inaba does not disclose or suggest combining together an N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region to form a semiconductor thin film resistor unit, as required by independent claim 4." (Brief, p. 8). Appellant also argues that "Kim does not disclose or suggest the step of combining together N-type and P-type thin film resistors to form a semiconductor thin film resistor unit, as required by independent claim[s] 4 and 7." (Brief, p. 11). The Erdeljac and Inaba references disclose that persons of ordinary skill in the art would have recognized that the resistors can be connected in series and parallel to function as one unit. A person of ordinary skill in the art would have reasonably expected that the N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region could have been combined together.

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The Appellant has presented arguments directed to the Erdeljac, Inaba and Kim considered individually rather than to the combination of the stated references. These arguments are not persuasive because obviousness cannot be rebutted by attacking references individually where the rejection is based upon the teachings of a combination of references. A reference must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole. *In re Merck & Co.*, 800 F.2d 1091, 1097, 231 USPQ 375, 380 (Fed. Cir. 1986).

Appellant argues that the Examiner's rejection is premised on hindsight. (Brief, p. 13). We are not convinced by Appellant's argument. The present record indicates that a person of ordinary skill in the art would have recognized that the pairing of resistors is generally known. A person of ordinary skill in the art would have reasonably expected that the N-type thin film resistor having a low resistance region and a P-type thin film resistor having a low resistance region, as described by Erdeljac, could have been combined together as suggested by the Examiner. It is well settled that a reference stands for all of the specific teachings thereof as well as the inferences one of ordinary skill in this art would have reasonably been expected to draw therefrom, see *In re Fritch*, 972 F.2d 1260, 1264-65, 23 USPQ2d 1780, 1782-83 (Fed. Cir. 1992); *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968).

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Appellant argues, Reply Brief, page 3, that Inaba does not disclose connecting together resistors to form a semiconductor thin film resistor unit and the resistors of Inaba are not combined together to form a single, distinct part or object (i.e., a unit) as required by the independent claims.

Appellant's argument is not persuasive. The present record does not support Appellant's argument. The specification discloses the resistance value is provided as one unit based on the combination of the N-type thin film resistor and P-type thin film resistor. (Specification, pp. 3 and 5). There is no indication that this combination must be separate from other resistors. Moreover, as pointed out by the Examiner, Answer page 5, Inaba discloses that the resistors can be connected in series and parallel to function as one unit. There does not appear, nor has Appellant contended, that other elements are ~~CONCLUSION~~ disclosure.

Based on our consideration of the totality of the record before us, having evaluated the *prima facie* case of obviousness in view of Appellant's arguments we conclude that the subject matter of claims 2-10 would have been obvious to a person of ordinary skill in the art from the combined teachings of the cited prior art. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

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Time for taking action

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

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ROMULO H. DELMENDO)	
Administrative Patent Judge)	
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JEFFREY T. SMITH)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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