

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HOWARD L. KALTER, H. BERNHARD POGGE, GEORGE S. PROKOP
and DAVID L. WHEATER

Appeal No. 2003-2137
Application No. 09/236,183

ON BRIEF

Before KIMLIN, GARRIS, and WALTZ, Administrative Patent Judges.
WALTZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's final rejection of claims 4 through 9, which are the only claims pending in this application. We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellants, the invention is directed to a method of testing chip functionality by depositing one additional layer of passivation and one layer of sacrificial metal, with the test circuitry in the kerf with the connections at the sacrificial metal

level, and final removal of the passivation and sacrificial metal layers after testing (Brief, pages 2-3).¹

According to appellants, all of the claims stand or fall together (Brief, page 4). Accordingly, pursuant to the provisions of 37 CFR § 1.192(c)(7)(2000), we select claim 4 from the grouping of claims and decide the ground of rejection in this appeal on the basis of this claim alone. Representative independent claim 4 is reproduced below:²

4. A method of [sic, testing] integrated circuit chips, comprising the steps of:

forming an insulating layer over an integrated circuit chip;
selectively opening at least one area over existing vias;

forming a test circuit in kerf areas adjacent to the chip prior to separating the chip from other chips formed on a semiconductor wafer;

depositing a sacrificial metal layer over the insulating layer and filling the at least one selectively opened area, the sacrificial layer in direct contact with the integrated circuit chip;

patterning the deposited sacrificial metal layer to form at least one direct connection between the test circuit and an exposed via;

¹We refer to the Brief filed June 3, 2002, Paper No. 14, as reinstated by the Request dated Dec. 10, 2002, Paper No. 17.

²We note that the copy of claim 4 from the Appendix to appellants' Brief is incorrect.

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testing the integrated circuit chip with the test circuit;

removing substantially all of the sacrificial metal layer and removing the insulating layer.

The examiner has relied upon the following references as evidence of obviousness:

Ahmad et al. (Ahmad)	5,483,175	Jan. 09, 1996
Beckenbaugh et al. (Beckenbaugh)	5,593,903	Jan. 14, 1997

The claims on appeal stand rejected under 35 U.S.C. § 103(a) as unpatentable over Ahmad in combination with Beckenbaugh (Answer, page 3).³ We reverse the examiner's rejection essentially for the reasons stated in the Brief and those reasons set forth below.

OPINION

The examiner finds that Ahmad discloses test circuitry within the chip area, forming conductive traces 21 and 22, and removing the sacrificial metal layer 21 by a planarization technique (Answer, page 3). The examiner recognizes that Ahmad does not disclose providing test circuitry in kerf areas adjacent to the chip prior to separating the chip from other chips on the semiconductor wafer, patterning the deposited sacrificial metal layer to form at least one connection, and scribing the wafer in

³The examiner has withdrawn the final rejection of claims 4-9 under 35 U.S.C. § 112, ¶1 (Answer, page 3).

the kerf areas to separate the chip and remove the test circuits (*id.*).

The examiner applies Beckenbaugh for its teaching of a chip testing method which includes forming test circuitry in the kerf area, forming an insulating layer 110 over the integrated circuit chip, patterning a sacrificial metal layer 120/130 in direct contact with the integrated circuit chip via bonding pad 78, forming at least one direct connection between the test circuit and an exposed via, scribing the wafer in the kerf areas to separate the chip, and removing the test circuits and insulating layer (Answer, pages 3-4). From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in the art "to provide the test circuitry specifically in the kerf areas and pattern the sacrificial metal layer as taught by Beckenbaugh et al. in practicing the testing process of Ahmad et al." Answer, page 4.

In our review of the examiner's obviousness analysis, we must first correctly construe the claim to define the scope and meaning of each contested limitation. See *Gechter v. Davidson*, 116 F.3d 1454, 1457, 1460 n.3, 43 USPQ2d 1030, 1032, 1035 n.3 (Fed. Cir. 1997). During examination proceedings, claims are given their broadest reasonable interpretation consistent with the specification. See *In re Graves*, 69 F.3d 1147, 1152, 36 USPQ2d

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1697, 1701 (Fed. Cir. 1995). Claim 4 on appeal requires that the sacrificial metal layer is "in direct contact" with the integrated circuit chip.

Appellants argue that an important difference between claim 4 on appeal and the references is that the claim requires the sacrificial layer to be in direct contact with the integrated chip while the sacrificial layer of the references does not touch or is not in "direct contact" with the integrated chip (Brief, pages 6-7). The examiner finds that metal layer 120 of Beckenbaugh is a sacrificial metal layer that is in "direct contact" with the integrated circuit chip "via bonding pad (78)" (Answer, page 3). Implicitly, the examiner construes the term "in direct contact" to include intervening structures such as the bonding pad 78. We disagree.

As argued by appellants in reply to the examiner's rejection under paragraph one of section 112 (now withdrawn), basis for the term "in direct contact" may be found in the specification at page 4, l. 32-page 5, l. 15, as well as Figures 6A-6C (Brief, pages 4-5; see also Paper No. 6 and the Answer, page 3). The specification teaches that a sacrificial metal layer is deposited on the surface of the insulator layer (page 2, ll. 21-22), thus necessarily filling the opened vias and contacting or touching the integrated

circuit chip. See the specification at page 4, ll. 2-8, where openings 12 are filled with a metal to form vias 26 connected to the selected vias 11. Accordingly, giving the term "in direct contact" its ordinary meaning, as illustrated by the specification and drawings, we construe this term as requiring the sacrificial metal layer to touch the integrated circuit chip.

The examiner argues that Ahmad shows a single conductive trace 21 formed over the chip being "in direct contact" with the integrated circuit chip (Answer, page 4). However, Ahmad teaches that the conductive traces 21 and 22 are "deposited over a passivation layer" (col. 5, ll. 49-50), and thus are not in "direct contact" with the integrated circuit chip as the claim has been construed above.

The examiner also argues that the conductive barrier layer 120 of Beckenbaugh is also a "sacrificial metal layer" in direct contact with the integrated circuit chip (Answer, page 4). We note that the conductive etch-barrier layer 120 of Beckenbaugh is not a required layer (col. 5, ll. 35-38). Regardless, sacrificial metal layer 130 (or 120) is in direct contact with bonding pad 78 (see Figure 5 and col. 4, l. 60-col. 5, l. 18), and thus is not "in direct contact" with the integrated circuit chip 20 as this term has been construed above.

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Additionally, we note that the examiner has not established any reasoning for the proposed modification of the references, i.e., the examiner has failed to present any motivation or reasoning for incorporating the features of Beckenbaugh in the testing process of Ahmad (Answer, page 4). See *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

For the foregoing reasons and those set forth in the Brief, we agree with appellants that the examiner's rejection is not well founded. Accordingly, we reverse the examiner's rejection of claims 4-9 under 35 U.S.C. § 103(a) over Ahmad in combination with Beckenbaugh.

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The decision of the examiner is reversed.

REVERSED

EDWARD C. KIMLIN)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
BRADLEY R. GARRIS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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THOMAS A. WALTZ)	
Administrative Patent Judge)	

TAW/jrg

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

