

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALBERTO O. ADAN

Appeal No. 2003-0886
Application No. 09/466,845

HEARD: NOVEMBER 5, 2003

Before THOMAS, RUGGIERO, and LEVY, Administrative Patent Judges.
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 2, 4, 5, 16, and 17¹. Claims 3 and 6-15 have been canceled.

BACKGROUND

Appellant's invention relates to a semiconductor device with bit lines formed via diffusion over word lines. An understanding

¹ The amendment (Paper No. 12, filed May 28, 2002) submitted subsequent to the final rejection has not been entered by the examiner (Paper No. 13, mailed June 7, 2002).

of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. A semiconductor device comprising:

an insulating film, a plurality of word lines parallel to one another, a gate insulating film and a first conductivity type semiconductor layer that are formed in this order;

wherein the surface of said insulating film is rendered flat with respect to the surface of said word lines, and said first conductivity type semiconductor layer includes parallel bit lines each comprising a second conductivity type high concentration impurity diffusion layer crossing said word lines, and

wherein on at least one of the bit lines a salicide film is formed on and in contact with the surface of said second conductivity type high concentration impurity diffusion layer.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Hirano	5,652,159	Jul. 29, 1997
Kapoor	5,780,350	Jul. 14, 1998
Chen et al. (Chen)	5,828,113	Oct. 27, 1998

Claims 1, 4, and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Hirano.

Claims 2, 16, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Hirano and further in view of Kapoor. Rather than reiterate the conflicting viewpoints advanced by the examiner and appellant regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 16, mailed November 20, 2002) for the examiner's complete

reasoning in support of the rejections, and to appellant's brief (Paper No. 15, filed August 23, 2002) and reply brief (Paper No. 18, filed January 16, 2003) for appellant's arguments thereagainst. Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellant's arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

Upon consideration of the record before us, we reverse, essentially for the reasons set forth by appellant. We begin with the rejection of claims 1, 4, and 5 under 35 U.S.C. § 103(a) as unpatentable over Chen in view of Hirano. We observe at the outset that appellant asserts (brief, page 3) that claims 1, 4,

and 5 stand or fall together. Consistent with this statement, appellant's arguments are directed to claim 1. Accordingly, we consider claim 1 to be representative of this group.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness.

Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

The examiner's position (answer, page 4) is that Chen does not teach a salicide film formed on and in contact with the surface of the source/drain regions. To overcome this deficiency in Chen, the examiner turns to Hirano for a teaching of a salicide layer 108 formed on and in contact with the surface of the surfaces of source/drain regions. The examiner asserts (id.) that it would have been obvious to have incorporated the salicide layer as taught by Hirano on and in contact with the surface of the source/drain regions in Chen in order to reduce the contact resistances for the transistor.

Appellant asserts (brief, pages 5 and 6) that providing Chen with the salicide layer of Hirano would result in Chen's functionality being destroyed. Specifically, appellant argues (brief, page 6) that if Chen's gate insulating film 48 were

formed over Hirano's silicide² film, the heat needed to form the gate insulating film would cause the silicide film to metalize in the form of islands which would degrade the performance of the silicide layer, possibly resulting in short circuiting between the bit lines 44 and the gate electrodes 50. It is further argued (brief, page 6) that the examiner's reason for making the modification i.e., to reduce contact resistances, would not happen due to the metalization of the silicide layer. It is additionally argued (brief, page 7) that Chen relates to a double density MROM, having bitlines and wordlines. Appellant asserts (id.) that in MROMS, source and drain electrodes are not needed, and that Hirano is directed to a liquid crystal display (LCD), which requires source drain electrodes. In Hirano, the source/drain electrodes are made up of silicide layer 108 and metal layer 109. Because Chen does not need source/drain electrodes, there is no need for the silicide layer 108 or metal layer 209 in Chen.

From our review of Chen, we find that Chen is directed to a double density MROM (col. 1, lines 1 and 2). As shown in figure 8, substrate 32 has a substantially flat surface. An insulation

² Appellant and the examiner appear to refer to silicide and salicide interchangeably. Throughout the Decision, we have used the terms in a manner consistent with their usage by the examiner and appellant.

layer 34 of field oxide covers the top surface of substrate 32. Bottom cell wordlines 36 extend over insulation layer 34 and are physically isolated from each other by first isolation strips 38 of oxide. Bottom gate dielectric 40 of oxide covers bottom cell wordlines 36 and first isolation strips 38. Polysilicon layer 42 completely covers bottom gate dielectric 40. Heavily doped regions 44 are formed into thin polysilicon film 40, and serve as conductive bitlines 44. On the bottom surface of polysilicon film 42, channel regions of thin film bottom cell transistors 46 (figure 7B) are formed directly above bottom cell wordlines 36 and between adjacent bitlines 44. Bitlines 44 serve as the source and drain electrodes for bottom cell memory transistors 46, whereas bottom cell wordlines 36 serve as gate electrodes for bottom cell memory transistors 46. Top gate dielectric 48 of oxide completely covers polysilicon layer 42 and the bitlines 44, which have been formed into polysilicon layer 42. Conductive polysilicon strips 50 are formed over top gate dielectric 48, and serve as top cell wordlines (col. 7, lines 37 through col. 8, line 8). By forming memory cell transistors on both the top and bottom surfaces of thin film polysilicon 42 in an alternating fashion, the MROM doubles the storage density of a conventional, prior art MROM (col. 8, lines 37-42). From the disclosure of

Chen, we find that although Chen is directed to an MROM including wordlines and bitlines, Chen does not disclose the use of a silicide layer formed on and in contact with the surface of the second conductivity type high concentration impurity diffusion layer (bitlines).

Turning to Hirano, we find that Hirano is directed to a technique for forming a thin film transistor (TFT) which is widely used in an active matrix type of liquid crystal device (LCD) (col. 1, lines 13-16). The TFT has a stable silicide layer formed apart from a channel region (col. 1, lines 9 and 10). As shown in prior art figure 1F, relied upon by the examiner, silicide layer 108 directly contacts the channel region of I-layer 104 (col. 2, lines 54-56). As a result, over etching of the lower layer 104 cannot be avoided (col. 2, lines 64 and 65). An object of the invention is to provide a TFT with a short channel length, so that direct contact between the I-layer 104 and the silicide layer is prevented (col. 4, lines 38 and 39). Hirano discloses (col. 5, lines 13-17) "forming source and drain electrodes, each of said source and drain electrodes comprising a metal silicide layer formed in a surface portion of the semiconductor film and a metal portion apart from the first mask section." As shown in figure 3C, a Cr silicide layer 8 is formed

at the interface between the I-layer 4 and the Cr film using mutual diffusion of the I-layer and the Cr film. Subsequently, a part of the non-reaction Cr film patterned such that the Cr film is separated from the end portions of the Cr silicide layers 8 on the channel region side. The separated Cr films are used together with the Cr silicide film layer 8 to constitute source and drain electrodes 9. As shown in figure 10E, as a result of implantation, the source and drain regions 11 are formed around the Cr silicide layers 8 in the I-layer 4 (col. 11, lines 17-19). In addition, Hirano discloses that the Cr silicide layers 8 are formed at the interface between the I-layer 4 and the Cr film using reaction of the I-layer and the Cr film (col. 11, line 64 through col. 12, line 2). From the disclosure of Hirano, we find that the silicide layer is used in the formation of the source and drain electrodes, and agree with appellant that because Hirano uses the silicide layer in the formation of source and drain electrodes, and because of the different structures disclosed by Chen and Hirano, we find no teaching or suggestion of adding the silicide layer between the bitlines 44 and top gate dielectric layer 48 of Chen.

We are not persuaded by the examiner's assertion (answer, page 4) that modifying Chen in view of Hirano's teachings would

result in reduced contact resistances for the transistor. In view of Chen's double density MROM structure having bitlines and wordlines, we agree with appellant (brief, page 6) that if a silicide layer were added above the bitlines 44, that when the top gate dielectric 48 were then added, the heat from the process would cause the silicide layer to be degraded. In addition, we find no teaching or suggestion in the references to provide the silicide layer of a transistor for an active matrix LCD into a double density MROM structure. From all of the above, we find that the examiner has failed to establish a prima facie case of obviousness of claim 1. Accordingly, the rejection of claims 1, 4, and 5 under 35 U.S.C. § 103(a) is reversed.

We turn next to the rejection of claims 2, 16, and 17 under 35 U.S.C. § 103(a) as unpatentable over Chen in view of Hirano and further in view of Kapoor. Turning to independent claim 16, we find that claim 16 requires, inter alia, "wherein in at least one of the bit lines a silicide film is formed on and in contact with the surface of said second conductivity type high concentration impurity diffusion layer but not on the surface of said adjacent low concentration impurity diffusion layers."

The examiner's position (answer, page 5) is that Chen "does not teach that second conductivity type low concentration

impurity diffusion layers are formed adjacent to and between the second conductivity type high concentration impurity diffusion layers on the first conductivity type semiconductor layer." The examiner (answer, page 5) relies upon Hirano for a teaching of a silicide layer in contact with the source and drain regions, and asserts (answer, page 6) that "Kapoor discloses a transistor structure comprising: a first conductivity type semiconductor layer (2); second conductivity type high concentration impurity diffusion layers (26 and 38, source/drain regions) formed in the layer (2); second conductivity type low concentration impurity diffusion layers (56 and 58, LDD regions) formed in the layer (2) adjacent to and between the second conductivity type high concentration impurity diffusion layers. See Kapoor's Fig. 8."

The examiner asserts (id.) that it would have been obvious to incorporate the LDD regions of Kapoor into Chen's transistor to reduce the electric field, which migrates short channel effects, reduces hot-carrier generation, and increases the junction breakdown voltage.

Appellant asserts (brief, page 9) that the source/drain silicide contacts 46, 48 and metal contacts 76, 78 of Kapoor are not required or needed in Chen, and that because Chen does not need the contacts, there would have been no reason as to why an

artisan would have provided the silicide contacts 46, 48 of Kapoor in the memory structure of Chen. It is further argued (id.) that there is no disclosure in the art for providing an LDD structure in an MROM such as Chen.

From our review of Kapoor, we agree with appellant. Chen is directed to a MOSFET with an improved LDD structure. As shown in figure 6, Kapoor discloses silicide source/drain contacts 46, 48, and titanium silicide contact 42 formed over gate electrode 12 (col. 5, lines 22-26). After spacers 30 are removed, (figure 7) implantation of the lightly doped drains (LDD) occurs. However, although Kapoor discloses the use of silicide source and drain contacts and an LDD region, we find no teaching or suggestion that would have motivated an artisan to provide the silicide source/drain contacts in the double density MROM of Chen. We agree with appellant that Chen has no need for the silicide contacts or LDD of structure of Kapoor, and find that the examiner has used appellant's disclosure as a template to reconstruct appellant's invention. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721

F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)).

Because Chen has no need for Kapoor's salicide contacts 46 and 48, and Kapoor does not address the issue of providing an LDD in a MROM, we are not persuaded that teachings from the applied prior art would appear to have suggested the claimed limitations. Thus, we find that Kapoor does not make up for the deficiencies of the basic combination of Chen and Hirano, and that the examiner has failed to establish a prima facie case of obviousness of claims 2, 16, and 17. Accordingly, the rejection of claims 2, 16, and 17 under 35 U.S.C. § 103(a) is reversed.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1, 2, 4, 5, 16, and 17 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
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