

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAZUO TANIGUCHI
and MASAHARU YOSHIMORI

Appeal No. 2003-0450
Application 09/394,039¹

HEARD: July 17, 2003

Before HAIRSTON, BARRETT, and BARRY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 2-11, 13, and 19-30. Dependent

¹ Application for patent filed September 13 1999, entitled "Method and Circuit for Enabling a Clock-Synchronized Read-Modify-Write Operation on a Memory Array," which is a division of Application 08/905,565, filed August 4, 1997, now U.S. Patent 5,996,052, issued November 30, 1999, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Application P08-218843, filed August 20, 1996.

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claims 21, 25, and 29 have been indicated to be allowable (examiner's answer, p. 9). Claims 5, 10, and 27 were amended by amendment after final rejection (Paper No. 15) pursuant to the examiner's recommendation (examiner's answer, Paper No. 19, p. 9). Since the examiner noted that claim 5, and presumably claim 10, would be allowable if amended (examiner's answer, p. 9), we assume that the amendment overcomes the rejection of claims 5 and 10 although the examiner makes no mention of this in the communication (Paper No. 17) noting entry of the reply brief and the amendment. Since the examiner only noted a problem with the language of claim 27 and did not say that it would be allowed if amended, we assume that claim 27 still stands rejected.

We reverse.

BACKGROUND

The disclosed invention relates to a semiconductor memory device capable of performing a high speed read modify write operation. Separate pins (or data buses) are provided for reading data from memory and writing data to memory. An input address is input to a read address decoding means to address the memory for reading and is also input to an address delay means, such as a first-in first-out (FIFO) buffer. The address is delayed for a predetermined number of clock cycles and becomes the write address which is decoded by a write address decoding

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means. Thus, data is read from a location, modified, and written back into the original location at a later time.

Claim 2 is reproduced below.

2. A semiconductor memory enabling a read modify write operation of data, comprising:

a memory cell array including a plurality of memory cells arranged in a matrix and able to be written with [sic, to?] and read;

a read address decoding means for independently decoding an address of a read memory cell in response to a first designated address;

a write address decoding means for independently decoding a write address of a memory cell in response to a second designated address;

a data reading means for reading data of a memory cell addressed by said decoded read address in said read address decoding means;

a data writing means for writing data to a memory cell addressed by said decoded write address in said write address decoding means; and

an address delay means by which said decoded write address decoded by said write address decoding means is delayed by a predetermined time from a read address decoded by said read address decoding means, said predetermined time being set as a predetermined plurality of times of basic synchronization pulse periods so that the data read modify write operation is accomplished in a pipeline manner by said basic synchronized pulse.

The examiner relies on the following references:

Kaneko et al. (Kaneko)	4,740,923	April 26, 1988
Hyatt	5,602,999	February 11, 1997
(entitled to a priority date of at least December 2, 1988)		

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Claims 2-4, 6-9, 11, 13, and 19-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaneko and Hyatt.²

We refer to the final rejection (Paper No. 7) (pages referred to as "FR__") and the replacement examiner's answer³ (Paper No. 19) (pages referred to as "EA__") for a statement of the examiner's rejection, and to the second appeal brief (Paper No. 12) (pages referred to as "Br__") and reply brief (Paper No. 17) (pages referred to as "RBr__") for a statement of appellants' arguments thereagainst.

OPINION

Initially, we note that the examiner interprets statements made by appellants in the description of Kaneko as the arguments of what is not taught by Kaneko and Hyatt (EA9-10). While we agree with the examiner that various statements in appellants' description of Kaneko (Br8-11) refer to limitations that are not in the claims, these are not appellants' arguments as to the patentability of the claims. Thus, all we have to go on to address appellants' arguments is the statement of the rejection.

² As noted at the beginning of the opinion, we assume that appellants' amendment overcomes the rejection of claims 5 and 10.

³ The initial examiner's answer (Paper No. 13) entered March 13, 2002, was indicated to be defective in a remand order (Paper No. 18) entered July 29, 2002, because it did not indicate that an appeal conference had been held. A replacement examiner's answer (Paper No. 19) indicating an appeal conference was entered December 17, 2002.

Appellants argue that Kaneko and Hyatt fail to disclose "a read address decoding means for independently decoding an address of a read memory cell in response to a first designated address" and "a write address decoding means for independently decoding a write address of a memory cell in response to a second designated address," as recited in claim 2 (Br13).

The examiner finds that either AD1 or AD2 is a read address decoding means whenever a read address is directed to memory matrix M1 or M2, respectively, and that either AD1 or AD2 is a write address decoding means whenever a write address is directed to memory matrix M1 or M2, respectively (EA5).

Appellants do not rebut the examiner's position in their reply brief and, absent argument to the contrary, we consider the examiner's finding to be reasonable. The limitations of "a read address decoding means for independently decoding" and "a write address decoding means for independently decoding" do not require separate, dedicated read and write decoding means as disclosed in Figs. 5 and 6, and do not preclude two decoding means that decode both read and write addresses as shown in Kaneko. The term "independently" is not defined in claim 2. While, perhaps, some argument could be made that the limitation of a "read modify write operation is accomplished in a pipeline manner" at the end of claim 2 somehow implies separate read and write decoding means which operate at the same time, this argument has not been made

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and that interpretation is not clear. Accordingly, the decoding means limitations are not grounds for distinguishing over Kaneko.

Appellants also argue that Kaneko and Hyatt fail to disclose "an address delay means by which said decoded write address decoded by said write address decoding means is delayed by a predetermined time from a read address decoded by said read address decoding means, said predetermined time being set as a predetermined plurality of times of basic synchronization pulse periods so that the data read modify write operation is accomplished in a pipeline manner by said basic synchronized pulse," as recited in claim 2 (Br13-14).

The examiner finds that DR1 and DR2 correspond to the claimed address delay means (EA6). The examiner states (EA6-7):

With regard to the final feature of claim 2, the address delay means, Kaneko et al. appears to introduce the delay to the operand data of a write request instead of the address data (as required by the invention). In the end, though, the result will be the same, since there is a delayed write operation which occurs in response to the passing of data through the delay register. In other words, the request cannot be fully serviced until both operand data and address data are received and delaying one or the other will yield a similar result. Applicant simply chose to delay the address data instead of the operand data.

Appellants argue that the examiner admits that Kaneko fails to explicitly teach the claimed address delay means (RBr6). It is argued that Kaneko fails to disclose delaying a decoded write address decoded by the write address decoding means (RBr6). As to the examiner's statement that delaying the address data will

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produce a similar result as delaying the operand data, appellants argue that this amounts to nothing more than personal conclusions unsupported by facts (RBr7-8).

As recognized by the examiner (at EA6), Kaneko does not delay the address, but delays the data. Thus, Kaneko fails to disclose the claimed subject matter. The examiner states that delaying the data rather than the address will yield the same result (EA6). This is not the test for obviousness because achieving the same result by different means may well be an unobvious improvement. Furthermore, Kaneko does not produce the same results as appellants' invention. Kaneko reads out data from an address a_0 and writes it to an address a_{0+n} (col. 1, line 31), that is, it shifts the address of the read-out data (col. 1, lines 66-67). Appellants' invention delays the address for a write for a predetermined number of clock cycles from a read address to coincide with write data, so that write modification is carried out to the same original address (specification, lines 20-21). Although appellants' invention could be used to shift the address of the read-out data, and delaying the write data by a time so that it is written to the same address that was read out is not claimed, it is a fact that the same thing is not going on in appellants' invention as in Kaneko because the claimed invention shifts address data. Figures 4B and 4C of Hyatt relied on by the examiner do not show

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delay of a write address with respect to a read address as claimed, and do not cure the deficiencies of Kaneko. We conclude that the examiner has failed to establish a prima facie case of obviousness with respect to independent claim 2. The rejection of claim 2 and its dependent claims 3, 4, and 6, is reversed.

Independent claims 7, 13, 19, and 24 recite address delay limitations similar to those in claim 2 and, for the reasons already stated with respect to claim 2, the rejection of claims 7, 13, 19, and 24 and their dependent claims 8, 9, 11, 20-23, and 25-30, is reversed.

CONCLUSION

The rejection of claims 2-4, 6-9, 11, 13, and 19-30 is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
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