The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAMA R. GORUGANTHU and MICHAEL R. BRUCE

Appeal No. 2003-0123
Application No. 09/383,781

ON BRIEF

Before HAIRSTON, BLANKENSHIP and JEFFREY T. SMITH, ***Administrative Patent Judges***.

JEFFREY T. SMITH, ***Administrative Patent Judge.***

DECISION ON APPEAL

Applicants appeal the decision of the Primary Examiner finally rejecting claims 1 to 13, 27 and 28.[1, 2] We have jurisdiction under 35 U.S.C. § 134.

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[1] In rendering our decision, we have considered Appellant's arguments presented in the Brief, filed May 2, 2002, and the Reply Brief filed September 10, 2002. We have considered the Examiner's position presented in the Answer, mailed July 30, 2002.

[2] Claims 14-26 have been withdrawn from consideration. (Paper no. 9, mailed August 21, 2001.

CITED PRIOR ART

As evidence of unpatentability, the Examiner relies on the following references:

Takemura et al. (Takemura)	5,786,242	Jul. 28, 1998
Jack et al. (Jack)	5,808,350	Sep. 15, 1998
Makita et al. (Makita)	5,851,860	Dec. 22, 1998
Ohtani et al. (Ohtani)	5,854,096	Dec. 29, 1998
Tanaka et al. (Tanaka)	6,008,101	Dec. 28, 1999
Nishida	6,014,965	Jan. 18, 2000

The Examiner has rejected claims 1 to 3, and 28 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita and Ohtani; claim 27 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita, Ohtani and Nishida; claim 4 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka and Takemura; and claims 5 to 13 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka, Takemura and Jack.

DISCUSSION

We have carefully reviewed the claims, specification and applied prior art, including all of the arguments advanced by both the Examiner and Appellants in support of their respective positions. This review leads us to conclude that the Examiner's § 103 rejections are not well founded. ***See In re Oetiker***, 977 F.2d

1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); ***In re Piasecki,*** 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984).

Rather than reiterate the conflicting viewpoints advanced by the Examiner and Appellants concerning the above-noted rejection, we refer to the Answer and the Brief and Reply Brief. Appellants' invention is directed to a method for providing an imaging path in a silicon surface that has been impaired by thinning. More specifically, Appellants' invention relates to a method for providing an imaging path in the backside of a semiconductor device such as a flip chip for subsequently obtaining an image of circuitry as viewed from the back side. (Specification p. 5). Claims 1, 4 and 9, which are representative of the claimed invention, appear below:

> 1. A method for providing an imaging path in a semiconductor device having a circuit side underlying silicon material, the method comprising:
>
> etching away some of the silicon material and forming a target surface; and
>
> laser-thermal annealing the silicon material by laser-scanning the target surface, and therein clearing a viewing path under the target surface.
>
> 4. A method for providing an imaging path that has been impaired by crystal defects formed as a result of applying a high temperature to the back side of the semiconductor device while thinning the back side

> using a laser at an energy level greater than or equal to a first energy level, the method comprising:
>
> scanning the back side of the semiconductor device using the laser applied at an energy level that is less than the first energy level and using the applied laser to reduce crystal defects.
>
> 9. For use with a semiconductor device having a circuit side and a back side, a method for obtaining images via the back side of the semiconductor device, the method comprising:
>
> laser-chemical etching the back side of the semiconductor device in vacuum and at a first power level;
>
> reducing the vacuum and scanning the back side of the semiconductor device using a laser operating at a power level that is less than the first power level; and
>
> using light to capture an image of a circuit through the back side of the semiconductor device.

The Examiner has rejected claims 1 to 3, and 28 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita and Ohtani; and claim 27 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita, Ohtani and Nishida.

Since we reverse the Examiner's rejection, we need to address only the independent claim, i.e., claim 1.

In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have

led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention. ***See, e.g., Heidelberger Druckmaschinen AG v. Hantscho Commercial Prods., Inc.,*** 21 F.3d 1068, 1072, 30 USPQ2d 1377, 1379 (Fed. Cir. 1994) (When the patent invention is made by combining known components to achieve a new system, the prior art must provide a suggestion, or motivation to make such a combination.); ***Northern Telecom v. Datapoint Corp.,*** 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990) (It is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor.); ***Uniroyal, Inc. v. Rudkin-Wiley Corp.,*** 837 F.2d 1044, 1044, 1051, 5 USPQ 1434, 1438 (Fed. Cir. 1988).

The method of claim 1 requires the treatment of the silicon layer, opposite the circuit side, to provide an imaging path to the underlying target circuit.

The Examiner asserts the subject matter of claim 1 is obvious over the combination of Makita and Ohtani. According to the Examiner, Makita discloses a method that comprises the etching of silicon material and forming a target surface. The Examiner asserts that Makita does not disclose the step of clearing a viewing path under the target surface. To remedy this deficiency the Examiner relies on

Ohtani. Ohtani discloses the use of a laser beam to recover the crystallinity in silicon that has been impaired by impurities such as implanted phosphorus ions. (Col. 14, ll. 13 to 29).

The combination of Makita and Ohtani fails to render the subject matter of claim 1 prima facie obvious. According to Appellant, Brief page 8, Makita is directed to etching layers of silicon used to form a gate layer and an active region in the circuit side of the device. Claim 1 requires the silicon that is being etched to be over an underlying circuit side. Neither Makita or Ohtani disclose etching silicon to provide an image path to the underlying circuit side. Neither Makita nor Ohtani is concerned with obtaining an image of underlying circuitry. The Examiner has not presented a reason to modify Makita to perform etching on the opposite side.

The Examiner asserts that Makita shows a gate electrode (106) below the silicon material layer (107). (Answer, p. 8). Makita discloses the oxide layer (107) acts as a mask that covers the gate electrode (106). Makita does not disclose etching this oxide layer to provide an image path for the gate electrode.

The Examiner added Nishida to the combination of Makita and Ohtani to reject the subject matter of claim 27.[3] However, Nishida does not remedy the

[3] Claim 27 is dependent on claim 1.

deficiency in Makita and Ohtani identified above. Thus, the rejection of claim 27 is reversed.

The Examiner rejected claim 4 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka and Takemura; and claims 5 to 13 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka, Takemura and Jack.

Tanaka's invention is directed to a manufacturing process for semiconductor devices integrated on a single substrate. The process includes the use of laser light that is selectively applied to the substrate at different illumination energies. The illumination energy is determined in accordance with the required semiconductor characteristics. (Col. 4, ll. 1-5). Tanaka discloses the reason why laser light illumination is performed in two steps is to minimize the degradation in uniformity of a film surface due to laser light illumination. (Col. 4, ll. 16-18). Tanaka discloses in the first illumination, the pixel area and the peripheral area are illuminated at the same energy without using a mask. In the second illumination, the pixel area and the peripheral circuit area are illuminated at different energies by using a mask. (Col. 5, ll. 1 to 13). The two-step illumination acts such that amorphous portions remaining in a film are crystallized in the first illumination and crystallization is accelerated over the entire film in the second illumination. As a

result, two kinds of crystalline silicon films having different crystallization processes are obtained. (Col. 5, ll. 18-28). Tanaka does not disclose the treatment of the backside of the semiconductor device.

Takemura discloses the manufacture of a semiconductor integrated circuit wherein the backside silicon is thinned by dry etching. (Col. 2, ll. 48-64). Takemura discloses that the etching is stopped prior to reaching the above laying silicon oxide layer to prevent damage to the device. (Col. 3, ll. 1-5). Takemura does not discuss thinning to provide an image path to the circuit layer.

The Examiner concludes, Answer page 5, "[i]t would have been obvious to one of ordinary skill in the art, at the time [of] invention[,] to modify Tanaka in view of Takemura by thinning the backside because it will help to improve the transparent optical property of the substrate. Further as the silicon substrate is thinned, the insulation performance of the substrate is enhanced (col. 2 lines 30-35 in Takemura '242 reference)."

The method of claim 4 requires scanning the back side of the semiconductor device using the laser applied at an energy level that is less than the first energy level and applied laser to reduce crystal defects. Tanaka discloses the two-step illumination acts such that amorphous portions remaining in a film are crystallized in the first illumination and crystallization is accelerated over the entire film in the

second illumination. (Col. 4, ll. 23-26). While the invention of Tanaka might be used on the back side of a semiconductor device, the Examiner has not provided motivation for such a modification. Neither Tanaka nor Takemura disclose the desirability of providing an image path to the underlying circuit side. Moreover, there is no indication that the two step illumination of Tanaka would provide the insulation property described by Takemura. The mere fact that the prior art could be modified would not have made the modification obvious unless the prior art suggested the desirability of the modification. ***In re Gordon,*** 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984); ***In re Laskowski,*** 871 F.2d 115, 117, 10 USPQ2d 1397, 1398 (Fed. Cir. 1989). The record indicates that the motivation relied upon by the Examiner suggesting the combination of Tanaka and Takemura came from the Appellants' description of the invention in the specification rather than from the applied prior art and that, therefore, the Examiner used impermissible hindsight in rejecting the claims. ***See W.L. Gore & Associates v. Garlock, Inc.,*** 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983); ***In re Rothermel,*** 276 F.2d 393, 396, 125 USPQ 328, 331 (CCPA 1960).

The subject matter of claim 9 requires laser-chemical etching the back side of the semiconductor device using two different power levels and using light to capture an image of the circuit through the back side of the semiconductor device. As stated

above, the Examiner has not provided motivation for using the two step illumination process of Tanaka on the backside of a semiconductor device.

The Examiner added Jack to the combination of Tanaka and Takemura to reject the subject matter of claims 5 and 13.[4] Neither Tanaka nor Takemura disclose etching silicon to provide an image path to the underlying circuit side. As stated above, the Examiner has not provided motivation for using the two step illumination process of Tanaka on the backside of a semiconductor device. Jack does not remedy this deficiency.

For the reasons stated above we reverse the Examiner's rejections under 35 U.S.C. § 103(a).

CONCLUSION

The rejections of claims 1 to 3, and 28 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita and Ohtani; claim 27 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Makita, Ohtani and Nishida; claim 4 as unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka and Takemura; and claims 5 to 13 as unpatentable

[4] Claims 5 and 13 are dependent on claim 4.

under 35 U.S.C. § 103(a) as obvious over the combination of Tanaka, Takemura and Jack are reversed.

REVERSED

KENNETH W. HAIRSTON ***Administrative Patent Judge***	)
HOWARD B. BLANKENSHIP ***Administrative Patent Judge***	) **BOARD OF PATENT APPEALS AND INTERFERENCES**
JEFFREY T. SMITH ***Administrative Patent Judge***	)

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