

UNITED STATES PATENT AND TRADEMARK OFFICE

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Ex parte YOAV HOLLANDER, LEV PLOTNIKOV, and YARON KASHAI

Appeal No. 2002-1305
Application No. 09/327,966

ON BRIEF

Before BARRETT, BARRY, and LEVY, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-20. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue on appeal concerns "design verification." Design verification is the process of determining whether a device under testing ("DUT") accurately implements requirements defined by a specification therefor. Design verification for a DUT may be done on the actual device or on a simulation model thereof; the invention focuses on the latter. (Spec. at 1.)

Verification via a simulation model is aided by the availability of hardware description languages such as Verilog and VHDL. These languages describe hardware at higher levels of abstraction than gates or transistors. (*Id.* at 2.) According to the appellants, however, these languages do not include features for testing the "temporal coverage" of the DUT, (*id.* at 4), i.e., the behavior of selected variables defining the DUT over time. Temporal coverage differs from automatic coverage, which is triggered by the appearance of a line of code or other static event, in that temporal coverage is driven by the occurrence of events in time. (*Id.* at 5.)

Accordingly, the appellants' invention tests the quality of a simulation model for a DUT through temporal coverage of the testing/verification process. Triggering events are determined according to fixed, predefined sampling times or according to occurrences of a temporal pattern of state transitions. Temporal data are collected during the process and analyzed to discern the behavior of selected variables and the quality of the simulation model for the DUT. More specifically, the data are searched for a "coverage hole," suggested by the absence of a particular value from a family of values. (*Id.* at 5-6.)

A further understanding of the invention can be achieved by reading the following claim.

1. A method for determining temporal coverage of a simulation model during a test verification process, the simulation model being constructed from a plurality of coverage items, the steps of the method being performed by a data processor, the method comprising the steps of:

(a) providing a coverage group for examining during the test verification process, said coverage group including at least one coverage item of the simulation model;

(b) providing a triggering event for determining when a state of said at least one coverage item of said coverage group is collected during the test verification process;

(c) detecting said triggering event;

(d) determining said state of said at least one coverage item as a collected coverage value; and

(e) determining the temporal coverage at least according to a set of said collected coverage values, such that a coverage hole is determined according to an absence of a particular state of said at least one coverage item in said collected coverage value.

Claims 1-6 and 8-20 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,937,765 ("Shupe"). Claim 7 stands rejected under 35 U.S.C. § 103(a) as obvious over Shupe and H.M. Sneed ("Sneed"), *State Convergence of Embedded Realtime Programs*, Proceedings of the Second Workshop on Software Testing, Verification, and Analysis, p. 245 (1988).

OPINION

Our opinion addresses the rejections in the following order:

- anticipation rejection of claims 1-6 and 8-20
- obviousness rejection of claim 7.

Anticipation Rejection of Claims 1-6 and 8-20

Rather than reiterate the positions of the examiner or the appellants *in toto*, we address a point of contention therebetween. The examiner interprets Shupe as follows.

The method of Shupe et al. comprises applying a set of **test vectors or patterns (i.e., coverage items)** to be used by a test verification program (i.e., coverage group) during fault simulation of an electronic circuit. Each of the test patterns in the program is converted into events, and each of the events is scheduled into **time slots (i.e., temporal triggering events)**. During the verification process, the results of the simulation are collected at each scheduled times of the events.

(Examiner's Answer at 4-5 (emphases added).) The appellants argue, "for the definition of triggering event to be the same as either the 'event' or the 'time slot' of Shupe, claim 1 would need to recite that the triggering event actually determines the state itself, not when the state is to be collected." (Appeal Br. at 8.)

"Analysis begins with a key legal question -- *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest

reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000).

Here, independent claim 1 specifies in pertinent part the following limitations: "(b) providing a triggering event for determining when a state of said at least one coverage item of said coverage group is collected during the test verification process; (c) detecting said triggering event; (d) determining said state of said at least one coverage item as a collected coverage value. . . ." Similarly, independent claim 16 specifies in pertinent part the following limitations: "(b) providing a triggering event in time determined according to a temporal expression, said temporal expression being constructed by the user, for determining when a state of said at least one coverage item of said coverage group is collected during the test verification process; (c) detecting said triggering event; (d) determining said state of said at least one coverage item as a collected coverage value. . . ." Also similarly, independent claim 19 specifies in pertinent part the following limitations: "(b) providing a triggering event for determining when a state of said at least one variable of said coverage group is collected during the test verification process; (c) detecting said triggering event; (d) determining said state of said at least one variable as a collected coverage value. . . ." Giving the independent claims their broadest, reasonable construction, the limitations require responding to a triggering event by determining a state of at least one coverage item.

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)).

Here, Shupe discloses "a 'two-pass' simulation algorithm employed by logic simulator 48 to apply the test program 46 to the circuit description 34 and execute the single-level fault simulation." Col. 12, ll. 39-42. "This [circuit] description 34 includes identification of the circuit elements and how they are interconnected." Col. 11, ll. 66-68. For its part, the "test program 46 compris[es] a set of test vectors or patterns to be applied to the primary inputs of circuit 36." *Id.* at ll. 7-9. "At the start of the logic simulation, the simulator 48 converts the test patterns in the program 46 into 'events' and schedules the events into a time wheel. The time wheel is divided into slots representing time steps. . . ." *Id.* at ll. 54-58.

"[T]here is no anticipation 'unless all of the same elements are found in exactly the same situation and united in the same way . . . in a single prior art reference.'" *Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894, 221 USPQ 669, 673 (Fed. Cir. 1984) (citing *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). Here, the examiner interprets the reference's test vectors as the claimed coverage items and Shupe's time slots as the claimed triggering events. (Examiner's Answer at 4-5.) To anticipate the claimed limitations based on these two interpretations, the reference would have to respond to its time slots by determining a state of at least one of its test vectors. Although Shupe does respond to the time slots by determining states, we are unpersuaded that the responsively determined states are those of the test vectors. To the contrary, the reference responds to its time slots by determining states of the circuit described by its circuit description 34. Specifically, a "state sampler 52 checks the state of every pin and thereby measures the sensitivity of each circuit element." Col. 12, ll. 31-33. Therefore, we reverse the anticipation rejection of claim 1 and of claims 2-6 and 8-18, which depend therefrom; of claim 16; and of claim 19 and of claim 20, which depends therefrom.

Obviousness Rejection of Claim 7

Turning to claim 7, the inquiry is whether the subject matter would have been obvious. "In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993)(citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "A *prima facie* case of obviousness is established when the teachings from the prior art itself would . . . have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, the examiner fails to allege, let alone show, that the addition of Sneed cures the aforementioned deficiency of Shupe. Absent a teaching or suggestion of responding to a triggering event by determining a state of at least one coverage item, we are unpersuaded of a *prima facie* case of obviousness. Therefore, we reverse the obviousness rejection of claim 7.

CONCLUSION

In summary, the rejection of claims 1-6 and 8-20 under § 102(b) and the rejection of claim 7 under § 103(a) are reversed.

REVERSED

LEE E. BARRETT
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

STUART S. LEVY
Administrative Patent Judge

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