

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SCOTT J. DEBOER, HUSAM AL-SHAREEF and RANDHIR THAKUR

Appeal No. 2002-1167
Application No. 09/089,445

ON BRIEF

Before OWENS, TIMM, and POTEATE, *Administrative Patent Judges*.
OWENS, *Administrative Patent Judge*.

DECISION ON APPEAL

This appeal is from the final rejection of claims 4-16, 18, 21-25, 27-29 and 36-39, and refusal to allow claims 17 and 30-35 as amended after final rejection. These are all of the claims remaining in the application.

THE INVENTION

The appellants claim a double sided lower electrode capacitor.
Claim 4 is illustrative:

4. A capacitor comprising:

a double sided electrode;

a first conductive layer in contact with an inner side of said double sided electrode;

a first dielectric layer in contact with said first conductive layer, said first dielectric layer located within the inner side of said double sided electrode;

a second dielectric layer in contact with an outer side of said double sided electrode and said first dielectric layer; and

a second conductive layer, wherein said dielectric layers are between said first conductive layer and said second conductive layer.

THE REFERENCES

Wu et al. (Wu)	5,786,250	Jul. 28, 1998 (filed Mar. 14, 1997)
Cho	5,817,555	Oct. 6, 1998 (filed May 2, 1997)
Zahurak et al. (Zahurak)	5,960,294	Sep. 28, 1999 (filed Jan. 13, 1998)
Kotecki et al. (Kotecki)	5,973,351	Oct. 26, 1999 (filed Jan. 22, 1997)

THE REJECTIONS

The claims stand rejected under 35 U.S.C. § 103 as follows:
claims 4, 5 and 10-13 over Cho in view of Zahurak; claims 4, 5,
9-11, 13-15 and 36-39 over Wu in view of Zahurak; and claims 6-8,
16-18 and 21-35 over Wu in view of Zahurak and Kotecki.

OPINION

We affirm the aforementioned rejections.

Appeal No. 2002-1167
Application No. 09/089,445

The appellants state that the claims stand or fall in four groups (brief, page 4). The only claims separately argued by the appellants, however, are claims 9 and 14 with respect to the rejection over Cho in view of Zahurak (brief, page 8), and claims 9 and 14 are not rejected over this combination of references. We therefore limit our discussion to one claim to which each rejection applies, i.e., claim 4 for the first two rejections and claim 23 for the third rejection. See *In re Ochiai*, 71 F.3d 1565, 1566 n.2, 37 USPQ2d 1127, 1129 n.2 (Fed. Cir. 1995); 37 CFR § 1.192(c)(7) (1997).

Rejections of claim 4 over Cho or Wu, in view of Zahurak

Cho discloses a capacitor (col. 1, line 8) comprising a double sided electrode (207), a first conductive layer (208) in contact with an inner side of the double sided electrode (figure 2F), a second dielectric layer (210) in contact with the first dielectric layer and the outer side of the double sided electrode (figure 2F), and a second conductive layer (211), wherein the second dielectric layer is between the first conductive layer and the second conductive layer (figure 2F). Cho does not disclose the appellants' first dielectric layer.

Wu discloses a capacitor (col. 1, line 11) comprising a double sided electrode (22), a first conductive layer (22a) in contact

with an inner side of the double sided electrode (figure 8), a second dielectric layer (32) in contact with the first dielectric layer and an outer side of the double sided electrode (figure 8), and a second conductive layer (34), wherein the second dielectric layer is between the first conductive layer and the second conductive layer (figure 8). Wu does not disclose the appellants' first dielectric layer.

The first conductive layers of both Cho (col. 3, line 9) and Wu (col. 8, line 21) are made of hemispherically grained (HSG) polysilicon. Both Cho (col. 3, lines 8-10) and Wu (col. 8, lines 12-30) indicate the HSG polysilicon has roughness which increases the surface area of the conductive layer. Zahurak teaches that in a capacitor, "[a] drawback to the use of rugged polysilicon is that the conductive grains thereof can become detached from an underlying semiconductor substrate during subsequent processing and can redeposit between memory cells, causing electrical shorts or double bit failures of adjacent memory cells" (col. 1, lines 57-62). The rugged polysilicon referred to by Zahurak can be HSG polysilicon (col. 4, lines 32-33). Zahurak conditions the surface of the rugged polysilicon by rapid thermal nitridization (RTN), thereby forming on the rugged polysilicon a thin film of silicon nitride (a dielectric layer) (col. 4, line 58

- col. 5, line 5). "The RTN step causes an increase in the strength of the rugged polysilicon of first conductive layer **20**, preventing grains of polysilicon from breaking apart during further processing and causing a short or double bit failure" (col. 5, lines 6-9).

Zahurak's disclosure of the benefit of RTN would have fairly suggested, to one of ordinary skill in the art, RTN of the HSG polysilicon first conductive layers of Cho and Wu to provide this benefit, i.e., increased strength of the rugged polysilicon of the first conductive layer which prevents grains of polysilicon from breaking apart during further processing and causing a short or double bit failure. As indicated by figure 2F of Cho and figure 8 of Wu, the RTN dielectric layer would be within the inner side of the double sided electrode.

The appellants argue that Zahurak strengthens his HSG polysilicon layer by RTN to prevent grain detachment from a substrate, whereas the HSG polysilicon layers of Cho and Wu are attached to an electrode rather than being attached to a substrate (brief, pages 7 and 9; reply brief, pages 2-4).

Zahurak teaches that "[i]n the context of this document, the term 'semiconductor substrate' is defined to mean any construction comprising semiconductive material, including but not limited to

Appeal No. 2002-1167
Application No. 09/089,445

bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials" (col. 1, line 62 - col. 2, line 2). This definition indicates that "semiconductor substrate" in the phrase "[a] drawback to the use of rugged polysilicon is that the conductive grains thereof can become detached from an underlying semiconductor substrate" includes a base semiconductor substrate having layers thereon. This interpretation is supported by Zahurak's disclosure that his HSG polysilicon layer (20) is attached to an insulative layer (12) which has been formed on a silicon substrate (11) (figure 1F).

Zahurak, therefore, would have fairly suggested, to one of ordinary skill in the art, applying his RTN to HSG polysilicon which has been formed on any layer on a base semiconductor substrate, such as the electrode layer of Cho or Wu. Accordingly, we affirm the rejections over Cho or Wu, in view of Zahurak.

*Rejection of claim 23 over
Wu in view of Zahurak and Kotecki*

Claim 23 requires that the double sided electrode is formed of a metal, wherein an oxide of the metal is conductive.

Appeal No. 2002-1167
Application No. 09/089,445

The examiner relies upon Kotecki (col. 1, lines 64-66) for a teaching that Ru and Ir, which are two of the appellants' electrode metals (specification, page 10, lines 20-26), and polysilicon, which is the disclosed electrode material of Wu (col. 7, line 35), are interchangeable as capacitor lower electrode materials (answer, page 7).

The appellants do not challenge the examiner's argument regarding the interchangeability of Ru, Ir and polysilicon as a capacitor lower electrode material. Instead, the appellants' rely upon the same argument with respect to claim 23 as was relied upon regarding claim 4 (brief, page 11). This argument is not persuasive for the reasons given above with respect to the rejection of claim 4 over Wu in view of Zahurak. Accordingly, we affirm the rejection over Wu in view of Zahurak and Kotecki.

DECISION

The rejections under 35 U.S.C. § 103 of claims 4, 5 and 10-13 over Cho in view of Zahurak, claims 4, 5, 9-11, 13-15 and 36-39 over Wu in view of Zahurak, and claims 6-8, 16-18 and 21-35 over Wu in view of Zahurak and Kotecki, are affirmed.

Appeal No. 2002-1167
Application No. 09/089,445

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

TERRY J. OWENS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
CATHERINE TIMM)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LINDA R. POTEATE)	
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Appeal No. 2002-1167
Application No. 09/089,445

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