

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

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*Ex parte* KENNETH E. MERRYMAN and RONALD G. ARNOLD

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Appeal No. 2001-2692  
Application No. 08/789,001

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ON BRIEF

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Before BARRY, BLANKENSHIP, AND SAADAT, *Administrative Patent Judges*.  
BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-38. The appellants appeal therefrom under 35 U.S.C. § 134(a). We affirm-in-part.

BACKGROUND

The invention at issue on appeal relates to implementing input/output ("I/O") functions for an integrated circuit ("IC"). Custom and semi-custom ICs are often designed by assembling predefined components, i.e., "macro cells" selected from a design library. (Spec. at 1.)

The appellants complain, however, that "[i]nterconnecting input, output, and bi-directional buffers can be time consuming and tedious, particularly if boundary scan or other test structures are included in the circuit design." (*Id.* at 2.) For board testing, a boundary scan path that includes each I/O buffer of an IC is provided. The path allows each I/O pad of the IC to be controlled and observed. (*Id.*)

Accordingly, the appellants' invention provides a user interface for receiving parameters from a circuit designer. Assembly rules, which define available I/O cells,<sup>1</sup> available boundary scan logic modules, and appropriate interconnections for various combinations thereof, are also provided. (*Id.* at 5.) A computer program selects and interconnects the I/O cells and the boundary scan logic modules to form interface modules. More specifically, the I/O cells and the boundary scan blocks are selected according to the parameters and are interconnected according to the rules. (*Id.* at 4-5.)

A further understanding of the invention can be achieved by reading the following claim.

1. A data processing system for automatically selecting and interconnecting a number of macro cells selected from a component library to form a first circuit design wherein each one of the number of

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<sup>1</sup>The cells are input, output, or bi-directional buffers. (Spec. at 5.)

macro cells has a number of terminals, the data processing system comprising:

- a. a user interface for receiving a number of user provided parameters;
- b. storing means for storing a predefined set of circuit design assembly rules; and
- c. assembly means coupled to said user interface and to said storing means for assembling the first circuit design in accordance with said number of user provided parameters and said predefined set of circuit design assembly rules.

Claims 1-38 stand rejected under 35 U.S.C. § 112, ¶ 1, as nonenabled.

Claims 1-35 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,918,614 ("Modarres") and by U.S. Patent No. 4,967,367 ("Piednoir"). The latter claims also stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,544,088 ("Aubertine").

#### OPINION

Our opinion addresses the rejections in the following order:

- nonenablement rejection of claims 1-38
- anticipation rejection of claims 1-35 by Modarres
- anticipation rejection of claims 1-35 by Aubertine
- anticipation rejection of claims 1-35 by Piednoir.

*Nonenablement Rejection of Claims 1-38*

Rather than reiterate the positions of the examiner or the appellants *in toto*, we address the main point of contention therebetween. The examiner alleges, "[t]here is no support for the 'automatically selecting and interconnecting' feature (see preamble, claim 1, for example). This applies to all independent claims. . . ." (Examiner's Answer at 4.) The appellants argue, "such a 'feature' is not found in claim 1," (Appeal Br<sup>2</sup> at 19); "it merely recites the purpose of a process or the intended use of a structure." (*Id.*)

"[T]he PTO bears an initial burden of setting forth a reasonable explanation as to why it believes that the scope of protection provided by that claim is not adequately enabled by the description of the invention provided in the specification of the application. . . ." *In re Wright*, 999 F.2d 1557, 1561-62, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (citing *In re Marzocchi*, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1971)). More specifically, "[t]o be enabling under §112, a patent must contain a description that enables one skilled in the art to make and use the claimed invention." *Atlas Powder Co. v. E. I. Du Pont de Nemours & Co.*, 750 F.2d 1569, 1576, 224 USPQ 409, 413 (Fed. Cir. 1984) (citing *Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 960, 220

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<sup>2</sup>We rely on and refer to the supplemental appeal brief, (Paper No. 11), in lieu of the original appeal brief, (Paper No. 8), because the latter was defective. (Paper No. 9.) The original appeal brief was not considered in deciding this appeal.

USPQ 592, 599 (Fed. Cir. 1983)). "That some experimentation is necessary does not preclude enablement; the amount of experimentation, however, must not be unduly extensive." *Id.* at 1576, 224 USPQ at 413.

Here, the examiner does not explain why he believes that the "automatically selecting and interconnecting" feature of independent claims 1, 35, 36, and 38 is not adequately enabled by the appellants' specification. Furthermore, he does not allege, let alone explain, that undue experimentation would be required to make and use the claimed invention. We will not "resort to speculation," *In re Warner*, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), as to such possible explanations. Therefore, we reverse the nonenablement rejection of claims 1-38.

*Anticipation Rejection of Claims 1-35 by Modarres*

"[T]o assure separate review by the Board of individual claims within each group of claims subject to a common ground of rejection, an appellant's brief to the Board must contain a clear statement for each rejection: (a) asserting that the patentability of claims within the group of claims subject to this rejection do not stand or fall together, and (b) identifying which individual claim or claims within the group are separately patentable and the reasons why the examiner's rejection should not be sustained." *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002 (citing 37

C.F.R. §1.192(c)(7) (2001)). "Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable." 37 C.F.R.

§ 1.192(c)(7) (2002). "If the brief fails to meet either requirement, the Board is free to select a single claim from each group of claims subject to a common ground of rejection as representative of all claims in that group and to decide the appeal of that rejection based solely on the selected representative claim." *McDaniel*, 293 F.3d at 1383, 63 USPQ2d at 1465.

Here, although the appellants allege "that pending claims 1-38 are patentably distinct from one another," (Appeal Br. at 16), they fail to satisfy the second requirement. More specifically, their pointing out differences in what claims 1, 4-27, and 31-35 cover, (*id.* at 28-43), is not an argument that the claims are separately patentable. Therefore, claims 4-27 and 31-35 stand or fall with representative claim 1.

With this representation in mind, rather than reiterate the positions of the examiner or the appellants *in toto*, we address the four points of contention therebetween. First, the examiner quotes "[c]ol. 6, lines 31-39" of Modarres. (Examiner's Answer at 14.) Observing that "[c]laim 1 is an independent apparatus claim limited to the combination of three (3) elements," (Appeal Br. at 28), the

appellants argue, "[t]he Examiner has not alleged that any of the prior art has any of this [sic] elements." (*Id.*)

"Analysis begins with a key legal question -- *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 1 specifies in pertinent part the following limitations:

- a. a user interface for receiving a number of user provided parameters;
- b. storing means for storing a predefined set of circuit design assembly rules; and
- c. assembly means coupled to said user interface and to said storing means for assembling the first circuit design in accordance with said

number of user provided parameters and said predefined set of circuit design assembly rules.

Giving the representative claim its broadest, reasonable construction, the limitations require assembling a circuit design in accordance with parameters provided by a user and predefined circuit design rules.

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "[A]nticipation is a question of fact." *Hyatt*, 211 F.3d at 1371, 54 USPQ2d at 1667 (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997)). "A claim is anticipated . . . if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)).

Here, Modarres explains that "[t]he preferred embodiment of [its] invention involves an automated system . . . which, given the total area of a chip, a hierarchy of functions, and a net list of the interconnections among terminal functions, places such functions within the chip so as to minimize the required area occupied by such functions and their interconnections, and to maximize the probability that such interconnections can be routed within that area." Col. 6, ll. 31-39. For our part, we find that the system assembles a circuit design in accordance with parameters provided by a user. Specifically, "the user specifies the 'root function' I-5 -- the function from which automatic placement should begin -- and the number of levels I-6 below the root function which the system should automatically place." Col. 8, ll. 46-50.

We further find that the assembly is also performed in accordance with several predefined circuit design rules. For example, "[a]s a default [rule], [the system] will place the clock in the center of the chip (in a vertical orientation), and will begin automatic placement at the top (chip) function and place functions throughout all levels of the hierarchy." Col. 9, ll. 34-38. Another example of a rule is that "[t]he system traverses the hierarchy in a 'preorder' (parent before children, as opposed to 'postorder,' children before parent) fashion. . . ." *Id.* at ll. 50-53. Furthermore, "[t]he system employs two methods to partition the children into two groups," col. 14, ll. 15-16. A predefined rule is used to select between the two methods. Specifically, "[t]he first

method, 'Exhaustive Partitioning' (illustrated in FIG. 5), is used if there are fifteen (the limit currently being used by the system) or fewer children to be placed in the parent." (*Id.* at ll. 22-25.) Therefore, we affirm the anticipation rejection of claim 1 and of claims 4-27 and 31-35, which fall therewith, by Modarres.

Second, observing that claim 2 "further limits the some [sic] of the macro cells," (Appeal Br. at 29), the appellants argue, "none of the prior art of record teaches this limitation." (*Id.*) They make a similar argument regarding claim 28. (*Id.* at 40.) Analogously, observing that claim 29 "further limits the macro cells," (Appeal Br. at 40), the appellants argue, "[t]he prior art of record does not contain this element." (*Id.*)

Claims 2 and 28 further specify in pertinent part the following limitations: "one or more of the number of macro cells are input macro cells." Analogously, claim 29 further specifies in pertinent part the following limitations: "one or more of the number of macro cells are output macro cells." Giving the claims their broadest, reasonable construction, claims 2 and 28 require at least one input, and claim 29 requires at least one output.

Turning to the reference, "a flip-flop" is among the components placed by the system of Modarres. Col. 1, l. 23. We find that the flip-flop inherently features inputs and outputs. "To establish inherency, the extrinsic evidence 'must make clear that the

missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (quoting *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991)). Here, because a flip-flop "has two **outputs**," M. Morris Mano ("Mano") *Computer System Architecture* 22 (3d ed. 1993) (emphasis added) (copy attached),<sup>3</sup> and "[t]he difference among various types of flip-flops is in the number of **inputs** they possess," *id.* (emphasis added), we find that inputs and outputs are necessarily present in the flip-flop of the reference. Therefore, we affirm the anticipation rejection of claims 2, 28, and 29 by Modarres.

Third, observing that claim 30 "further limits the macro cells to include bi-directional cells," (Appeal Br. at 41), the appellants argue, "[t]he prior art of record does not contain this combination." (*Id.*) For its part, claim 30 further specifies in pertinent part the following limitations: "one or more of the number of macro cells are bi-

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<sup>3</sup>Although references cannot be combined for anticipation, additional references may be used to interpret an anticipatory "reference and to reveal what it would have meant to one of ordinary skill at the time the invention was made." *Studiengesellschaft Kohle, m.b.H.v. Dart Indus., Inc.*, 726 F.2d 724, 726-27, 220 USPQ 841, 842 (Fed. Cir. 1984). Here, we use Mano to interpret Modarres and to reveal what the latter reference would have meant to one of ordinary skill at the time the invention was made

directional macro cells." Giving the claim its broadest, reasonable construction, the limitations require at least one bi-directional element.

Turning to the reference, the flip-flop of Modarres can input data via its aforementioned inputs and output data via its aforementioned outputs. Because the inputting and outputting occur in different directions, i.e., inward and outward, we find that the flip-flop is a bidirectional element. Therefore, we affirm the anticipation rejection of claim 30 by Modarres.

Fourth, observing that claim 3 "further limits some of the macro cells," (Appeal Br. at 29), the appellants argue, "[t]his limitation is not taught in any of the prior art of record. . . ." (*Id.*) For its part, claim 3 further specifies in pertinent part the following limitations: "selected ones of the input macro cells include a boundary scan logic module, said boundary scan logic module having a number of terminals."

"The review authorized by 35 U.S.C. Section 134 is not a process whereby the examiner . . . invite[s] the [B]oard [of Patent Appeals and Interferences] to examine the application and resolve patentability in the first instance." *Ex parte Braeken*, 54 USPQ2d 1110, 1112 (Bd.Pat.App. & Int. 1999). In an *ex parte* appeal, "the Board is basically a board of review — we review . . . rejections made by patent examiners." *Ex*

*parte Gambogi*, 62 USPQ2d 1209, 1211 (Bd.Pat.App. & Int. 2001). Furthermore, "absence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, the examiner does not allege, let alone show, that the reference discloses the aforementioned limitations. We will not resort to speculation as to such a possible disclosure. Therefore, we reverse the anticipation rejection of claim 3 by Modarres.

*Anticipation Rejection of Claims 1-35 by Aubertine*

We address the four points of contention between the examiner and the appellants. First, the examiner cites "col. 6, line 22 to col. 8, line 43" of Aubertine. (Examiner's Answer at 7.) Observing that "[c]laim 1 is an independent apparatus claim limited to the combination of three (3) elements," (Appeal Br. at 28), the appellants argue, "[t]he Examiner has not alleged that any of the prior art has any of this [sic] elements." (*Id.*) As construed in addressing the rejection by Modarres, claim 1 requires assembling a circuit design in accordance with parameters provided by a user and predefined circuit design rules.

Turning to the reference, Aubertine discloses "a method for physical layout of elements of a computer system by assigning I/O pins for physical package design. . . ." Col. 6, ll. 24-25. For our part, we find that the method assembles a circuit design in accordance with parameters provided by a user. Specifically, "the first step 1 of our method is an input from a user of the assignment method which defines or establishes net priorities." *Id.* at ll. 58-60. Also, "[s]tep 1 of the method begins with accepting as input the placement of all components at each system level and the logical association of all nets in accordance with top-down design." Col. 7, ll. 28-31.

We further find that the assembly is also performed in accordance with several predefined circuit design rules. For example, "[a] test is made to determine if the results of Step 3 are legal with respect to the lowest level component of the system. (Design information describing the placement of components with respect to other components across the system is used to make this determination.)" *Id.* at 7-11. The reference's design information is a rule.

Furthermore, [i]n selecting the component I/Os at the different levels of the system for assignment to nets, design constraints that are established for these nets must be obeyed." Col. 4, ll. 11-13. These design constraints are rules. One such rule is that "the wire length must be kept to a minimum." *Id.* at l. 21. Therefore, we affirm

the anticipation rejection of claim 1 and of claims 4-27 and 31-35, which fall therewith, by Aubertine.

Second, observing that claim 2 "further limits the some [sic] of the macro cells," (Appeal Br. at 29), the appellants argue, "none of the prior art of record teaches this limitation." (*Id.*) They make a similar argument regarding claim 28. (*Id.* at 40.) Analogously, observing that claim 29 "further limits the macro cells," (Appeal Br. at 40), the appellants argue, "[t]he prior art of record does not contain this element." (*Id.*) As construed in addressing the rejection by Modarres, claims 2 and 28 require at least one input, and claim 29 requires at least one output.

Turning to the reference, Aubertine describes its I/O pins as "[i]nput/[o]utput wires leading to or from a component of a computer system." Col. 1, ll. 21-22. Because the method of the reference assigns input wires and output wires, we find that it includes inputs and outputs. Therefore, we affirm the anticipation rejection of claims 2, 28, and 29 by Aubertine.

Third, observing that claim 30 "further limits the macro cells to include bi-directional cells," (Appeal Br. at 41), the appellants argue, "[t]he prior art of record does

not contain this combination." (*Id.*) As construed in addressing the rejection by Modarres, claim 38 requires at least one bi-directional element.

Because the method of Aubertine assigns input/output pins, we find that at least some of the pins are bi-directional. Therefore, we affirm the anticipation rejection of claim 30 by Aubertine.

Fourth, observing that claim 3 "further limits some of the macro cells," (Appeal Br. at 29), the appellants argue, "[t]his limitation is not taught in any of the prior art of record. . . ." (*Id.*) As construed in addressing the rejection by Modarres, claim 3 further specifies in pertinent part the following limitations: "selected ones of the input macro cells include a boundary scan logic module, said boundary scan logic module having a number of terminals."

The examiner does not allege, let alone show, however, that the reference discloses the aforementioned limitations. We will not resort to speculation as to such a possible disclosure. Therefore, we reverse the anticipation rejection of claim 3 by Aubertine.

*Anticipation Rejection of Claims 1-35 by Piednoir*

We address a point of contention between the examiner and the appellants. The examiner cites "col. 6, line 37 to col. 10, line 58" of Piednoir. (Examiner's Answer at 15.) Observing that "[c]laim 1 is an independent apparatus claim limited to the combination of three (3) elements," (Appeal Br. at 28), the appellants argue, "[t]he Examiner has not alleged that any of the prior art has any of this [sic] elements." (*Id.*) As construed in addressing the rejection by Modarres, independent claim 1 requires assembling a circuit design in accordance with parameters provided by a user and predefined circuit design rules. Claim 35, the other independent claim rejected by Piednoir, requires the same.

The examiner does not allege, let alone show, that the reference discloses assembling a circuit design in accordance with parameters provided by a user and predefined circuit design rules. We will not resort to speculation as to such a possible disclosure. Therefore, we reverse the anticipation rejection of claim 1; of claims 2-34, which depend therefrom; and of claim 35 by Piednoir.

"The PTO Rules of Practice require the examiner to cite only what he considers the 'best references.'" *E.I. duPont de Nemours & Co. v. Berkley & Co.*, 620 F.2d 1247, 620 F.2d 1247, 1266-67, 205 USPQ 1, 16 (8th Cir. 1980). "The examiner is not called

upon to cite *all* references that may be available, but only the 'best.'" M.P.E.P. § 904.03 (8th ed., rev. 1 Feb. 2003) (quoting 37 C.F.R. § 1.104(c)(2002)). "Multiplying references, any one of which is as good as, but no better than, the others, adds to the burden and cost of prosecution and should therefore be avoided." *Id.*

Here, the examiner's treatment of Piednoir evidences that the reference is no better than Modarres or Aubertine. The examiner should avoid such multiplication of references.

#### CONCLUSION

In summary, the rejection of claims 1-38 as nonenabled is reversed. The rejection of claims 1, 2, and 4-35 as anticipated by Modarres, and the rejection of the same claims as anticipated by Aubertine, are affirmed. In contrast, the rejection of claim 3 as anticipated by Modarres, the rejection of the same claim as anticipated by Aubertine, and the rejection of claims 1-35 as anticipated by Piednoir, are reversed.

"Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences. . . ." 37 C.F.R. § 1.192(a)(2002). Accordingly, our affirmance is based only on the arguments made in the brief. Any arguments or authorities not included therein are neither before us nor at

issue but are considered waived. No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

LANCE LEONARD BARRY	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
HOWARD B. BLANKENSHIP	)	APPEALS
Administrative Patent Judge	)	AND
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MAHSHID D. SAADAT	)	
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