

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte WAI LEE and TOSHIYUKI SAKUTA

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Appeal No. 2001-2593  
Application No. 09/074,197<sup>1</sup>

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ON BRIEF

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Before HAIRSTON, KRASS and SAADAT, Administrative Patent Judges.  
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 23 and 28. Claims 1-4, 12, 14, 16-22, 26, 27, 29 and 30 are withdrawn from consideration as being drawn to a non-elected invention, claims 6, 7, 10, 24 and 25 are allowed and claims 5, 8, 9, 11, 13 and 15 are cancelled.

We reverse.

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<sup>1</sup> Application for patent filed May 7, 1998, which is a divisional of the Application No. 08/426,349, filed April 21, 1995, now U.S. Patent No. 5,818,743.

BACKGROUND

Appellants' invention is directed to a digital multiplier for multiplying a plurality of multiplicands. An adder adds the intermediate results that are generated from the multiplicands while delay elements delay the arrival of at least one of the intermediate signals in order to synchronize the arrival of the signals in the adder circuit (specification, page 3).

Representative independent claim 28 is reproduced below:

28. A digital multiplier for multiplying signals and multiplier signals to produce final result signals, comprising:

means for generating a plurality of intermediate result signals from said multiplicand signals and from said multiplier signals, and placing said intermediate result signals on intermediate result signal lines;

a plurality of adder circuits receiving said intermediate result signal lines for adding said intermediate result signals to generate said final result signals; and

a plurality of unclocked delay elements placed in selected intermediate result signal lines so as to delay the arrival of some of said intermediate result signals so said adder circuits to synchronize the arrival of the signals input to said adder circuits and reduce spurious switching of said adder circuits.

The Examiner relies on the following references in rejecting the claims:

Goldschmidt et al (Goldschmidt)	3,515,344	June 2, 1970
Nash	4,811,270	Mar. 7, 1989

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Claims 23 and 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Goldschmidt.

Claims 23 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nash.

We make reference to the answer (Paper No. 19, mailed April 5, 2001) for the Examiner's reasoning, and to the appeal brief (Paper No. 17, filed February 5, 2001)<sup>2</sup> for Appellants' arguments thereagainst.

#### OPINION

With respect to the 35 U.S.C. § 102 rejection of the claims, Appellants argue that latch registers 43 and 51 of Goldschmidt, as characterized by the Examiner to be the same as the claimed unclocked delay elements, are clocked (brief, page 5).

Appellants point out that the recited unclocked delay elements synchronize the arrival of the intermediate result signals in the adder circuits and reduce spurious switching of the adder circuits (brief, page 4). Appellants further point to the description of latch registers 24-29 in Goldschmidt (Col. 4, lines 21-23) as the only description for a latch register and

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<sup>2</sup> The appeal brief was filed as a supplemental appeal brief to add a statement regarding the cancellation of claim 15, which was omitted in the originally filed appeal brief (Paper No. 15, filed October 4, 2000).

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conclude that latch registers 43 and 51 must be the same as latch registers 24-29 and are, therefore, clocked (brief, page 6).

In response, the Examiner points out that the latches in Goldschmidt do delay the input signals by a predetermined amount and are unclocked since no clock signals are disclosed (answer, page 5). The Examiner further argues that the fact that the latches are described as "gated" does not mean that they are clocked unless they are gated by a clock signal, which is not disclosed in Goldschmidt (id.).

A rejection for anticipation under section 102 requires that the four corners of a single prior art document describe every element of the claimed invention, either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation. See Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999); In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

After reviewing Goldschmidt, we agree with Appellants' assertion that the claimed unclocked delay elements, are not the same as the latch registers disclosed in the reference. Goldschmidt describes an adder for generating the final sum for a plurality of simultaneously applied operands (abstract and Col.

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1, lines 41-47). However, we remain unpersuaded by the Examiner's assertion that the absence of the description of a clock means that the latches are unclocked and further buttress our view by referring to Col. 5, lines 48-53 of Goldschmidt describing the structure of the disclosed latch registers to be the same as those disclosed in U.S. Patent No. 3,340,388.<sup>3</sup> A review of Patent No. 3,340,388 shows that the shift registers used in the adder of Goldschmidt are all clocked (col. 3, lines 33-39). As depicted in Figure 2 of Patent No. 3,340,388, the latching function is performed by storing the carry and sum outputs in a pair of clocked latches 30 and 40 and therefore, what the Examiner characterizes in Goldschmidt as unclocked delay elements, are actually clocked latch registers. Thus, since all the limitations of the appealed claims are not taught by the applied prior art, Goldschmidt cannot anticipate the claims. Accordingly, the 35 U.S.C. § 102 rejection of claims 23 and 28 is not sustained.

Turning to the 35 U.S.C. § 103 rejection of the claims, Appellants argue that Nash does not teach that delay elements 19 are unclocked and instead, describes the delay elements as one bit shift registers which are well-known to be clocked (brief,

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<sup>3</sup> The commonly owned U.S. Patent No. 3,340,388 to Earle, a copy of which accompanies this decision.

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page 7). Appellants point out that Nash, instead of the claimed synchronizing the arrival of the intermediate results signals in the adder circuit, uses a clocked delay signal (col. 5, lines 31-37) and is concerned with delaying the adder signals by at least one clock period (brief, page 7). Additionally, Appellants question the Examiner's reason for modifying Nash and using unclocked delay elements where the reference is not concerned with reducing spurious switching of adder circuits (id.).

The Examiner responds to Appellants' arguments by asserting that using unclocked delay elements in the adder of Nash would have been obvious since such elements are well known in the art and are used in Nash for synchronizing the inputs (answer, page 5). The Examiner further relies on the broad recitation of the delay elements being unclocked to conclude that such kind of delay elements are known in the art (id.).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). To reach a conclusion of obviousness under § 103, the examiner must produce a factual basis supported by teaching in a prior art reference or shown to be common knowledge of unquestionable demonstration. Our

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reviewing court requires this evidence in order to establish a prima facie case. In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). The Examiner must not only identify the elements in the prior art, but also show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead the individual to combine the relevant teachings of the references." In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Nash relates to a full adder circuit to be implemented in multi-bit digital multipliers or dividers (col. 1, lines 5-9). The multiplier includes an array of one-bit delay shift registers 19 that delay the eight-bit multiplicand and synchronize its arrival at the next row of the full adder (col. 3, lines 19-24 and Figure 1). However, as pointed out by Appellants (brief, page 7), Nash indicates that all of the circuit elements in Figure 1 are clocked (col. 5, lines 31-37) which means that the delay elements 19 are also clocked. Therefore, contrary to the Examiner's proposed modification of the clocked shift registers of Nash to use unclocked delay elements, we do not find any teaching or suggestion in Nash, nor, in Appellants' somewhat broad recitation of "an unclocked delay element" that supports the obviousness of the modification. The Examiner has further

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failed to establish how the delay elements of Nash that are positively disclosed to be clocked, may be substituted by unclocked delay elements, as recited in claims 23 and 28.

Based on our analysis above, we find that the Examiner has failed to set forth a prima facie case of obviousness because Nash neither teaches nor would have suggested to one of ordinary skill in the art using an unclocked delay element for delaying the fourth input by a predetermined time interval. Accordingly, we do not sustain the 35 U.S.C. § 103 rejection of claims 23 and 28 over Nash.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 23 and 28 under 35 U.S.C. §§ 102 and 103 is reversed.

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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	)	
MAHSHID D. SAADAT	)	
Administrative Patent Judge	)	

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