

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SCARLETT Z. WU, DARREN D. NEUMAN
AND ARVIND B. PATWARDHAN

Appeal No. 2001-2448
Application No. 09/105,492¹

ON BRIEF

Before BARRY, LEVY and SAADAT, Administrative Patent Judges.
SAADAT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-20, which are all of the claims pending in this application.

We reverse.

¹ Application for patent filed June 26, 1998.

BACKGROUND

Appellants' invention is directed to a decoding system that uses a memory arbitration scheme to combine the speed and responsiveness of hardware with the flexibility and efficiency of software and to improve the decoding system performance (specification, page 14). Dedicated logic devices issue "GO signals" for memory access which are fed into a first-in, first-out (FIFO) queue (specification, pages 16 & 17). Dequeue logic receives memory ready signals and asserts a DEQUEUE signal if the memory device is idle and therefore ready to handle a memory transaction (specification, page 17).

Representative independent claim 1 is reproduced as follows:

1. A decoding system comprising:

a memory storage device that stores data;

a plurality of decoding devices coupled to said memory storage device and which carry out memory transactions with the memory storage device;

a microcontroller coupled to said memory storage device and to said plurality of decoding devices, comprising:

a control logic device that issues a primary GO instruction associated with one of said decoding devices;
and

a FIFO that queues the primary GO instruction,

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wherein said one of said decoding devices accesses said memory storage device if the primary GO instruction is dequeued from said FIFO.

The Examiner relies on the following reference in rejecting the claims:

Kavipurapu	6,009,488	Dec. 28, 1999 (filed Nov. 7, 1997)
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Claims 1-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kavipurapu.

We make reference to the answer (Paper No. 16, mailed May 7, 2001) for the Examiner's reasoning in support of the rejection, and to the appeal brief (Paper No. 15, filed March 26, 2001) for Appellants' arguments thereagainst.

OPINION

Appellants argue that, among the elements cited in Kavipurapu, latch 201 is the only element that could arguably carry out memory transactions but question the way the Examiner characterizes other elements 201, 203, 205 as decoders that carry out memory transactions. Appellants also contest the Examiner's characterization of WRITE and SEARCH commands of Kavipurapu as the claimed GO instruction and indicate that neither command is queued or dequeued from a FIFO (brief, page 5). Appellants further point out that the disclosed WRITE and SEARCH signals are

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not stored in a queue or dequeued therefrom and are, in fact, used to control the operation of the queue (id.).

In response to Appellants' arguments, the Examiner asserts that Kavipurapu's elements 201, 203 and 205 are memory devices and inherently contain decoding circuitry (answer, page 9). The Examiner also points out that, since specific kinds of decoding devices and the memory transactions are not claimed, the operation of these elements of Kavipurapu in relation to the line cache 206 are characterized as "memory transactions" (answer, page 10). Furthermore, the Examiner relies on the teaching of the prior art that the request queue 202 operates in a FIFO manner (col. 9, lines 58-62) and concludes that the WRITE and SEARCH commands of Kavipurapu are put in the request queue which are dequeued in response to a control signal (answer, page 10).

Before addressing the Examiner's rejection based on prior art, it is essential that we understand the claimed subject matter and determine its scope. Accordingly, we will initially direct our attention to Appellants' claim 1 in order to determine its scope. Claim interpretation must begin with the language of the claim itself. See Smithkline Diagnostics, Inc. v. Helena Laboratories Corp., 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). See also Pitney Bowes, Inc. v. Hewlett-Packard Co.,

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182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999) ("The starting point for any claim construction must be the claims themselves.").

A review of claim 1 reveals that it is the primary GO instruction issued by the recited microcontroller that the claimed FIFO queues not the memory transaction requests issued by the recited decoding devices. Once the memory transaction is performed and one of the decoding devices accesses the memory storage, the FIFO further dequeues the primary GO instruction. Therefore, the FIFO queues and dequeues the memory grant signals or the GO instructions. Similarly, claims 7 and 13 require that the memory arbitration queue memory grant signals and dequeue a grant when a decoding device is to perform a memory transaction.

A rejection for anticipation under section 102 requires that each and every limitation of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994). See also Atlas Powder Co. v. Ireco Inc., 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1947 (Fed. Cir. 1999).

We observe that Kavipurapu, as depicted in figure 20, teaches that request queue 202 operates in a FIFO manner (col. 9, lines 58-62), but provides no disclosure related to memory grant

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queues. Figures 20-23 actually depict the receive and transmit link interface circuitry wherein the bus cycle of the processor is decoded to be either a read or write as the data and address information are latched (col. 9, lines 50-52). An appropriate header from header pool 207 as well as the address/data/control of the bus cycle is mapped to the packet as it is placed in request queue 202 (col. 9, lines 52-61). Therefore, what the Examiner takes for the queuing of the GO instructions is, in fact, queuing of the requests wherein either data is packetized and sent or data is sent to the memory controller for storage (col. 10, lines 17-31).

In view of the analysis above, we find that the Examiner has failed to meet the burden of providing a prima facie case of anticipation since, as discussed above, the computer system of Kavipurapu queues the requests instead of the claimed queuing and dequeuing of the GO or the memory grant signals. Accordingly, the rejection of claims 1, 7 and 13 as well as claims 2-6, 8-12 and 14-20, dependent thereupon, under 35 U.S.C. § 102 over Kavipurapu cannot be sustained.

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CONCLUSION

In view of the foregoing, the decision of the Examiner rejecting claims 1, 3, 4, 7, 9, 10, 12-24 and 27 under 35 U.S.C. § 102 is reversed.

REVERSED

LANCE LEONARD BARRY)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
STUART S. LEVY)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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MAHSHID D. SAADAT)	
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