

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN JAY MUNROE, SCOTT ALAN PLAETZER
and JAMES WILLIAM STOPYRO

Appeal No. 2001-1578
Application No. 08/771,550

ON BRIEF

Before BARRETT, FLEMING, and RUGGIERO, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-31, all the claims pending in the instant application.

The invention relates to computer operating systems which support multiple simultaneous tasks. See page 1 of Appellants' specification. As computers became more sophisticated, it became common for computer systems to execute multiple tasks concurrently. Operating systems designed for such computer systems were required to manage operations within the available

address space of the computer. See page 2 of Appellants' specification. Since the addresses needed typically exceeded the address space available in the processor's hardware, this was done by allocating a separate address space to each task, resulting in multiple virtual address spaces. See pages 2 and 3 of Appellants' specification. Figure 3 depicts at a high level the mapping of entities in virtual address space of a multi-tasking computer system utilizing a conventional multiple virtual address space operating system of the prior art. See page 15 of Appellants' specification. As shown in Figure 3, each task can map the entire virtual address space. Some entities, such as A, C, and L, are mapped in the address space of more than one task, but are not necessarily at the same virtual address. Other entities, such as D and P, exist only within a single task. Because the virtual address of a particular entity in the system of Figure 3 may vary from task to task, there is no persistent virtual address associated with an entity. See page 15 and 16 of Appellants' specification.

As an alternative to multiple virtual address space architecture, it is possible to utilize a single very large system address space, one which is sufficiently large that it is not necessary to have multiple overlapping virtual address

spaces, one for each task. See page 3 of Appellants' specification. Figure 4 depicts a high level mapping of entities in virtual address space of a computer system utilizing a single-level store architecture. As shown in Figure 4, there is but a single large virtual address space map 401, and all entities are mapped into this one space. See page 16 of Appellants' specification.

Figure 5 depicts a high level mapping of entities in virtual address space of a computer system utilizing a shared address space region architecture, according to the preferred embodiment of Appellants' invention. The SAS region 510 has characteristics of a single-level stored architecture. As in the case of the conventional multiple virtual address space architecture of Figure 3, regions outside of the SAS 510 allow each task to have its own mapping of identities to the virtual address space, multiple virtual address space. See pages 17 and 18 of Appellants' specification. Thus, Appellants' invention has the advantage of a single-level storage architecture and be compatible with code written for conventional multiple virtual address space architecture. See page 19 of Appellants' specification.

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Independent claim 1 present in the application is reproduced as follows:

1. A computer system, comprising:

a processor;

a memory;

an operating system for supporting concurrent execution of a plurality of tasks on said computer system, said operating system comprising a plurality of instructions executable on said processor, said plurality of instructions maintaining a plurality of data structures supporting operating system functions performed by said plurality of instructions executing on said processor;

wherein said operating system allocates a plurality of overlapping task virtual address spaces, each task virtual address space being allocated to a respective task;

wherein said operating system allocates, within a plurality of said task virtual address spaces, a shared address space region, said shared address space region occupying the same virtual address range within each respective task virtual address space, said shared address space region being less than the entire task virtual address space; and

wherein said operating system allocates, within said virtual address range occupied by said shared address space region, a plurality address ranges assigned to respective addressable entities, each respective one of said range of addresses being uniquely and persistently assigned to its respective addressable entity, and wherein the virtual address range of an addressable entity shared by two or more tasks resides at the same address within each task's shared address space region.

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References

The references relied on by the Examiner are as follows:

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| Magee et al. (Magee '710) | 5,729,710 | Mar. 17, 1998 (filed Jun. 22, 1994) |
| Magee et al. (Magee '383) | 5,771,383 | Jun. 23, 1998 (effectively filed Dec. 27, 1994) |
| Alderson | 5,347,649 | Sep. 13, 1994 |

J. Chase, et al. "Sharing and Protection in a Single-Address-Space Operating System," ACM Transactions on Computer Systems, Vol. 12, No. 4, (11-1994), pp. 271-301.

Rejections at Issue

Claims 1-4, 9-13, 16-18, 23, 24, 27 and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Magee '383 and Magee '710 in view of Chase.

Claims 5-8, 14, 15, 19-22, 25, 26 and 29-31 stand rejected under 35 U.S.C. § 103 as being unpatentable over Magee '383 and Magee '710 in view of Chase and further in view of Alderson.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief and answer for the respective details thereof.

OPINION

With full consideration being given to the subject matter on appeal, the Examiner's rejections and the arguments of Appellants

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and the Examiner, for the reasons stated *infra*, we reverse the Examiner's rejection of claims 1-31 under 35 U.S.C. § 103.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed. Cir. 1992). *See also In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. *Oetiker*, 977 F.2d at 1445. 24 USPQ at 1444. *See also Piasecki*, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and arguments." *In re Oetiker*, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board

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must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." *In re Lee*, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and Examiner.

Appellants argue that the Examiner improperly rejected their claims as being obvious over Magee '383 and Magee '710 and Chase, because there is no teaching or suggestion in the references to combine the two addressing schemes disclosed. See page 11 of the brief. In particular, Appellants agree that Magee '383 and Magee '710 are classical multiple virtual addressed space systems. By the same token, Appellants agree that Chase is a universal address space system. However, Appellants argue that there is no suggestion that the classical multiple virtual address space system disclosed in Magee '383 and Magee '710 be grafted onto a universal address space system of Chase to produce Appellants' claimed invention. See page 12 of the brief.

The Examiner's reason for making the combination is that in doing so, sharing is improved without sacrificing protection.

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The Examiner points to page 275, first paragraph of Chase. See page 5 and 8 of the answer.

When determining obviousness, "the [E]xaminer can satisfy the burden of showing obviousness of the combination 'only by showing some objective teaching in the prior art or individual to combine the relevant teachings of the references.'" ***In re Lee***, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002), ***citing In re Fritch***, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'" ***In re Dembiczak***, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617. "Mere denials and conclusory statements, however, are not sufficient to establish a genuine issue of material fact." ***Dembiczak***, 175 F.3d at 999, 50 USPQ2d at 1617, ***citing McElmurry v. Arkansas Power & Light Co.***, 995 F.2d 1576, 1578, 27 USPQ2d 1129, 1131 (Fed. Cir. 1993).

Upon our review of Chase, we fail to find that Chase suggests or teaches to those skilled in the art to provide a combination of multiple virtual address spaces with Chase's single universal address space. Chase clearly teaches that the single address space operating system is superior to the

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conventional multiple virtual address operating system. In particular, on page 277, Chase states that the familiar model of programs as independent short-lived processes that transform a stream of input to a stream of output is needlessly restrictive and forces poor structuring and performance tradeoffs for a broad and increasingly important class of applications. Chase further goes on to say that these applications are better served by the single-address-space structure. We find no suggestion or teaching in Chase to support the Examiner's proposed combination. Therefore, we will not sustain the Examiner's rejection of claims 1-4, 9-13, 16-18, 23, 24, 27 and 28 under 35 U.S.C. § 103 as being unpatentable over Magee '383 and Magee '710 in view of Chase. Furthermore for the rejection of claims 5-8, 14, 15, 19-22, 25, 26, and 29-31 we note that the Examiner relies on the above rationale for this combination as well. Therefore, we will not sustain this rejection either.

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In view of the foregoing, we have not sustained the
Examiner's rejection of claims 1-31 under 35 U.S.C. § 103.

REVERSED

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| LEE E. BARRETT |) | |
| Administrative Patent Judge |) | |
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| |) | BOARD OF PATENT |
| MICHAEL R. FLEMING |) | APPEALS |
| Administrative Patent Judge |) | AND |
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| JOSEPH F. RUGGIERO |) | |
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