

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD CLIFF

Appeal No. 2001-0149
Application No. 08/896,001

ON BRIEF

Before FLEMING, GROSS and BLANKENSHIP, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-18.

The invention relates to a interconnect chip for programmable logic devices. The interconnect chip (108) is coupled to a programmable logic device (102) by connectors (114).

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Connectors (110) couple interconnect chip (108) to the horizontal network of conductors, while connectors (112) couple interconnect chip (108) to the vertical network of conductors. See Appellant's Specification, page 5, lines 4-10 and associated figure 1.

Independent claim 1 present in the application is representative and reproduced as follows:

1. A system comprising:

a plurality of programmable logic devices configured in an array;

horizontal conductors for interconnecting logic devices in rows in the array;

vertical conductors for interconnecting logic devices in columns in the array; and

an interconnect chip associated with each logic device and coupled to an associated logic device and to a vertical and horizontal conductor.

References

The references relied on by the Examiner are as follows:

Winlow	5,263,149	Nov. 16, 1993
Mooney et al. (Mooney)	5,515,440	May 7, 1996
Terrill et al. (Terrill)	5,642,262	June 24, 1997

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Rejections at Issue

Claims 1-16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Winlow in view of Terrill.

Claims 17 and 18 are rejected under 35 U.S.C. § 103 as being unpatentable over Winlow and Terrill as applied to claims 1-16 above, and further in view of Mooney.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Brief¹ and the Answer for the respective details thereof.

OPINION

With full consideration being given the subject matter on appeal, the Examiner's rejections and the arguments of Appellant and Examiner, for the reasons stated *infra*, we reverse the Examiner's rejection of claims 1-18 under 35 U.S.C. § 103.

The Examiner states that Winlow discloses a system comprising a plurality of programmable logic devices (element

¹The Appellant filed an appeal brief, Paper No. 11, on April 26, 2000. The case was remanded to the Examiner on June 10, 2002. The Appellant filed an amended appeal brief, Paper No. 14, on July 16, 2002. We will refer to the amended appeal brief as simply the brief. The Examiner's Answer, Paper No. 15, was mailed on July 26, 2002.

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1(a) in claim 1); an interconnect chip for coupling first and second programmable logic devices (element 1(d) in claim 1). See Examiner's Answer, page 3, lines 16-19.

Appellant argues that the Examiner has not provided a sufficient basis for rejecting the claims. Appellant asserts that the Examiner's arguments in the Final Office Action do not take into account all the limitations of the claims. Appellant states that the only independent claims in the application, claims 1, 7, 10 and 17, variously include distinctions such as an "interconnection chip associated with each logic device" designed to provide communication of information between logic devices in the same row or column. See Brief, page 3, lines 15-18.

In rejecting claims under U.S.C. § 103, the Examiner bears the initial burden of establishing a *prima facie* case. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed. Cir. 1992). ***See also In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ at 1444. ***See also Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

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The factual inquiry must "be based on objective evidence of record." *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). This "showing must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." *Lee*, 277 F.3d at 1344, 61 USPQ2d at 1434. With these principles in mind, we commence review of the pertinent evidence and arguments of Appellant and Examiner.

The Examiner argues that Winlow teaches a programmable interconnect logic block in which the programmable logic devices and the programmable interconnect logic block are programmable logic arrays. Further, the Examiner argues that the final office action addresses the arguments of the limitations that recite an array of logic devices in that the cited prior art of Winlow teaches an array of one column and multiple rows. Furthermore, the Examiner refers to the teaching of arrays as cited in the Applicant's Admitted Prior Art (AAPA). See Examiner's Answer, page 7, lines 6-14.

However, as pointed out by our reviewing court, we must first determine the scope of the claim. “[T]he name of the game is the claim.” *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). In addition, claims are to be interpreted as the terms reasonably allow. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Independent claims 1, 7, 10, and 17 recite an “interconnect chip associated with each logic device” designed to provide communication of information between logic devices in the same row or column. Taking a reasonably broad interpretation, claims 1, 7, 10, and 17 require the interconnect chip to provide communication of information between logic devices in the same row or column.

Upon review, the Examiner has not shown that Winlow teaches an “interconnect chip associated with each logic device” designed to provide communication of information between logic devices in the same row or column as recited in claims 1, 7, 10, and 17. Winlow teaches a system comprising a plurality of programmable logic devices. However, the interconnection structure as disclosed in Winlow comprises only of programmable

logic devices in a single column. Winlow does not include a design of the interconnect chips coupled to an associated logic device and to a vertical and horizontal conductor. Further, Winlow fails to teach that the interconnect chip is associated with each logic device in the array on a one-to-one basis.

In addition, there is no suggestion of arranging the programmable logic devices in an array which are coupled by horizontal conductors and vertical conductors. While arrays of programmable logic devices are well known in the art and the concept of connecting the element of an array by horizontal and/or vertical conductors is also well known, there is no suggestion to lead a person of ordinary skill in the art to connect an interconnect chip associated with each logic device in the array on a one-to-one basis and then connect vertical conductors to the logic devices in rows in the array and horizontal conductors to the logic devices in columns in the array.

In conclusion, we find the Winlow reference fails to disclose, teach or suggest an "interconnect chip associated with each logic device" designed to provide communication of

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information between logic devices in the same row or column as recited in claims 1, 7, 10, and 17. Since claims 2-6, 8-9, 11-16, and 18 are dependent on independent claims 1, 7, 10, and 17, we also cannot sustain the art rejections of these claims. Therefore, we cannot sustain the rejection of claims 1-18 under 35 U.S.C. § 103.

REVERSED

MICHAEL R. FLEMING)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ANITA PELLMAN GROSS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

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