

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRISTOPHER McCALL and PETER JUERGEN KLIM

Appeal No. 2000-2228
Application No. 09/067,153

ON BRIEF

Before JERRY SMITH, BARRY, and BLANKENSHIP, *Administrative Patent Judges*.
BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-3, 5, and 9. The appellants appeal therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The appellants' invention concerns "self-timed logic circuits." A self-timed circuit operates asynchronously on the concept of demand; it operates only when requested. Responding to such a request, the circuit generates outputs according to its internal scheduling, presents the results to the requestor, and then "goes to sleep" to await a subsequent request.

Because most self-timed circuitry is dynamic, explain the appellants, it is prone to errors from noise. (Spec. at 4.) Furthermore, routing a clocking signal to each dynamic circuit increases design complexity and clock loading. (*Id.* at 5.) Static circuits, in contrast, do not suffer from many drawbacks of dynamic circuits. Given enough time, static circuits can recover from an incorrect evaluation; a correct state can be gained by waiting. Furthermore, static circuits require no clock signals, which reduces design complexity and clock loading. (*Id.*) Dynamic circuits, however, consistently outperform static circuits in terms of delay. (*Id.* at 6.)

Although static and dynamic circuits can be swapped for one another without concern in a typical clocked system, the appellants assert that the use of static circuits is not as simple in a self-timed system. (*Id.*) They explain that interlocking created by using dynamic circuits in a self-timed system is lost when those circuits are replaced with static circuits. (*Id.* at 6-7.)

The appellants' add that their invention permits static circuits to be used in a self-timed system, thereby attaining the benefits of static logic. (*Id.* at 8.) More specifically, Figure 3 of their specification shows a self-timed logic circuit 300 featuring a first transparent latch register 301 to receive one or more input data signals from one or more sources. A control circuit 304 receives one or more valid signals corresponding

to each of the input data signals. Combinatorial static logic 302 then receives the input data signals from the first register and performs at least one function on the input data signals. A second transparent latch register 303 receives the output from the combinatorial static logic block, and the control circuit clocks the output data signals through the second register to at least one sink.

A further understanding of the invention can be achieved by reading the following claim:

1. A self-timed logic circuit comprising:

a first transparent latch register operable for receiving one or more input data signals from one or more sources;

a control circuit operable for receiving one or more valid signals, wherein each one of the one or more valid signals is associated with a particular input data signal;

a combinatorial static logic block comprising one or more static logic circuits, wherein the control circuit clocks the one or more input data signals from the first transparent latch register to the combinatorial static logic block when all of the one or more valid signals are received by the control circuit, wherein the combinatorial static logic block produces one or more output data signals; and

a second transparent latch register operable for receiving the one or more output data signals.

Claims 1-3, 5, and 9 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,565,798 ("Durham").

OPINION

Rather than reiterate the positions of the examiner or appellants *in toto*, we address the main point of contention therebetween. The examiner asserts, "Durham teaches DATA signals which are evaluated by Self Resetting domino logic (SR) circuits and clocked through a series of SR circuits along with an AND circuit (see Fig. 4)." (Examiner's Answer at 5.) The appellants argue, "Durham teaches that SR circuits 402 produce a DATA OUT signal and not merely 'clocked-through' DATA signals." (Reply Br. at 4.) The examiner responds, "[t]here is no basis to appellant's argument that claim 1 specifically and clearly recites the these DATA signals are directly connected to the AND circuit without any evaluation or modification from the first transparent latch register." (Examiner's Answer at 5.)

"Analysis begins with a key legal question -- *what is the invention claimed?*" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). Here, independent claim 1 specifies in pertinent part the following limitations: "the control circuit clocks the one or more input data signals from the first transparent latch register to the combinatorial static logic block. . . ." Accordingly, the claim requires that a control circuit cause data to be transferred from a transparent latch register to a combinatorial static logic block without the data being modified.

“[H]aving ascertained exactly what subject matter is being claimed, the next inquiry must be into whether such subject matter is novel.” *In re Wilder*, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)). “[A]bsence from the reference of any claimed element negates anticipation.” *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Here, the examiner equates, (Examiner’s Answer at 5), the claimed control circuit with Durham’s “macro 402, which in this embodiment includes 10 rows of self-resetting domino logic.” Col. 3, ll. 47-49. “Data from register 401 [are] received by macro 402,” col. 3, l. 47, explains the reference, and the macro outputs “data that [are] transmitted to . . . AND circuit 404.” *Id.* ll. 56-58. The data output from the macro to the AND circuit, however, are not the same (unmodified) data received by the macro. To the contrary, the appellants, who are also Durham’s inventors, avow “that the SR

circuits 402, which comprise a plurality of domino logic rows (see, Figs. 5A and 5B) do not merely pass through the received DATA signals from register 401, but perform domino logic operations on those DATA signals so that they are not the same DATA signals when outputted as DATA_OUT.” (Appeal Br. at 5.) The reference supports their avowal by two implications. First, an explanation that “[m]acro 402 receives the incoming data and **produces** output data that is transmitted to . . . AND circuit 404,” col. 3, ll. 56-58 (emphasis added), implies that the macro modifies the incoming data. Second, a labeling of the incoming data, viz., “INPUT₁, INPUT₂, and INPUT₃,” Fig. 5A, differently from the output data, viz., “DATA_OUT,” Fig. 5B, implies the same.

The examiner’s failure to show a control circuit that causes data to be transferred from a transparent latch register to a combinatorial static logic block without the data being modified negates anticipation. Therefore, we reverse the rejection of claim 1 and of claims 2, 3, 5, and 9, which depend therefrom.

CONCLUSION

In summary, the rejection of claims 1-3, 5, and 9 under § 102(b) is reversed.

REVERSED

JERRY SMITH
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

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