

The opinion in support of this decision is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TYSON TUTTLE et al.

Appeal No. 2000-1259
Application No. 08/815,894

ON BRIEF

Before MARTIN, JERRY SMITH, and FLEMING, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 43, 44, and 52-63, all of the pending claims. We reverse.

A. The invention

The invention is a sampled amplitude read channel for reading user data and embedded servo data in a magnetic disk storage device, and is more particularly directed to a sampled amplitude read channel that permits a reduction, during recording, of the size of the physical gaps formed between adjacent sectors. Specification at 13, ll. 13-21. Referring to

Figures 2A and 2B, each radial servo spoke 17 on the disk contains recorded servo control information consisting of a preamble 5 to allow the gain control circuitry to acquire the read signal, a servo sync mark 7 to signal the beginning of the servo data, and the servo data 3. Id. at 9, 11. 3-10. The specification further explains that "[s]imilar to the servo data sectors, the user data sectors 15 also comprise an acquisition preamble 68 and a sync mark 70 to signal the beginning of a user data field 72 as shown in Figure 2B." Id. at 10, 11. 3-5.

The prior-art sampled amplitude read channel illustrated by Appellants' Figure 1 includes a gain control circuit 50, a timing recovery circuit 28, a DC offset circuit 1, and a discrete time sequence detector 34. Appellants' brief explains that the gain control, timing recovery, and DC offset circuits are decision-directed feedback loops whose coefficients are adjusted depending on whether the read channel is reading a preamble field or a data field. Brief at 2. Specifically, when reading the preamble field, the loop bandwidth is increased to provide a fast transient response in order to minimize the time and number of bits required to obtain the preamble field; when reading the data field, the loop bandwidth is decreased to attenuate noise and gain variance. Id. at 2-3. Furthermore, the discrete time sequence detector comprises a large buffer for storing a survivor

sequence associated with a trellis, with the result that the output of the sequence detector is delayed by the length of this buffer. Id. at 3. Prior-art read channels wait for the sequence detector to finish processing a current sector before changing the loop coefficients of the gain control, timing recovery, and DC offset circuits, thereby necessitating that the sectors be separated by a physical gap which is long enough to account for the latency in the sequence detector:

Before the read channel can process a new user or servo data sector, components such as the filters in timing recovery, gain control, and DC offset control must be reconfigured to acquire the preamble of the new sector. During this reconfiguration process, the magnetic disk continues to spin under the read head[,] creating [the need for] a physical gap on the medium between the end of a current sector and the beginning of a new sector.

Specification at 21, l. 22 to p. 22, l. 4. Appellants' sampled amplitude read channel, shown in Figure 3, reduces the size of the required gap by using the following pipelining technique:

In order to reduce the gap between sectors, operation of the read channel is pipelined by reconfiguring the gain control 50, timing recovery 28, the DC offset 1 circuits before the discrete time equalizing filter 26 and sequence detector 34 have finished processing the samples for the current sector. This allows the read channel to begin acquiring the preamble (68,5) of a next sector (user or servo data) concurrent with processing the end of the previous sector, thereby decreasing the [required] physical gap on the medium between sectors.

Id. at 22, ll. 4-12.

The claims

Claim 43 is representative:

43. A sampled amplitude read channel for reading data recorded on a magnetic disk medium by detecting digital data from a sequence of discrete time sample values generated by sampling pulses in an analog read signal from a magnetic read head positioned over the magnetic disk medium, the magnetic disk medium comprising a plurality of concentric data tracks wherein a data track comprises a plurality of sectors, the sampled amplitude read channel comprising:
- (a) a discrete time timing recovery circuit for synchronizing the discrete-time [sic, discrete time] sample values to a baud rate of the data recorded on the magnetic disk medium;
 - (b) a discrete time gain control circuit for adjusting an amplitude of the analog read signal relative to a desired partial response; and
 - (c) a discrete time sequence detector for detecting an estimated data sequence from the sequence of discrete time sample values;
- wherein the timing recovery circuit and the gain control circuit are reconfigured before the discrete time sequence detector finishes processing the discrete time sample values of a current sector so that the read channel can begin acquiring an acquisition preamble of a next sector, thereby reducing a physical gap between sectors on the magnetic disk medium.

The rejections and references

The rejections are based on the following U.S. patents.

Petersen	5,463,603	Oct. 31, 1995 (filed Jan. 29, 1993)
Dudley et al. (Dudley)	5,583,706	Dec. 10, 1996 (filed Nov. 17, 1994)

Claims 43, 44, 52-54, and 57-61 stand rejected under 35 U.S.C. § 102(e) as anticipated by Petersen.

Claims 43, 44, and 52-63 stand rejected under § 102(e) as anticipated by Dudley.

The merits of the rejections

Dudley's Figure 1 shows what Dudley describes as a conventional sampled amplitude recording channel, which includes a variable gain amplifier 22 and a sampler 24 which are controlled by gain and timing control circuit 28. Also included is a discrete time sequence detector 34. Comparing Appellants' claim 43 to this figure, the claimed discrete timing recovery circuit reads on sampler 24 and gain and timing control circuit 28, the claimed discrete time gain control circuit reads on variable gain amplifier 22 and gain and timing control circuit 28, and the claimed discrete time sequence detector reads on discrete time sequence detector 34.

Dudley's Figure 3, on which the examiner specifically relies, shows Dudley's sampled amplitude read channel, which is similar to the Figure 1 channel in that it, too, includes a variable gain amplifier 22, a sampler 24, a gain and timing control circuit 28, and a discrete time sequence detector 34, with the result that the aforementioned claim limitations read on the Figure 3 read channel in the same way as on the Figure 1 read channel. Although not important insofar as claim 43 is concerned, the Figure 3 channel additionally includes a DC offset control circuit G100.

Regarding claim 43's requirement that the timing recovery circuit and the gain control circuit be reconfigured before the discrete time sequence detector finishes processing the discrete time sample values of a current sector so that the read channel can begin acquiring an acquisition preamble of a next sector, the examiner states that

Figure 3 of Dudley et al[.] shows the parallel pipeline processing of gain and timing control information. See element 28. This continual adjustment of the adaptive device of Dudley et al[.] occurs before, during, and after data sector detection to continuously reconfigure the device of Dudley. See column 7, lines 43-60 of Dudley et al.

Answer at 5-6. This argument is unconvincing because the cited passage (reproduced below) appears to be describing the gain and timing adjustments performed by the operation of the gain control

and timing control circuits rather than the reconfiguration of those circuits (i.e., alteration of their operational parameters):

The equalized sample values 32 are applied over line 27 to decision-directed gain and timing control 28 for adjusting the amplitude of the read signal and the frequency and phase of the sampling device 24, respectively. Timing recovery adjusts the frequency of sampling device 24 over line 23 in order to synchronize the equalized samples 32 to the waveform (see co-pending U.S. patent application Ser. No. 08/313,491 entitled "Improved Timing Recovery For Synchronous Partial Response Recording"). Gain control adjusts the gain of variable gain amplifier 22 over line 21. The equalized samples $Y(n)$ 32 are sent to a discrete time sequence detector 34, such as a maximum likelihood (ML) Viterbi sequence detector, to detect an estimated binary sequence $\hat{b}(n)$ 33. An RLL decoder 36 decodes the estimated binary sequence $\hat{b}(n)$ 33 into estimated user data 37. In the absence of errors, the estimated binary sequence $\hat{b}(n)$ 33 is equal to the recorded binary sequence $b(n)$ 8, and the decoded user data 37 is equal to the recorded user data 2.

(Emphasis added.) Dudley, col. 7, ll. 43-60. Furthermore, even assuming for the sake of argument that this passage is referring to configuring the gain control and timing control circuits in one way while reading the preamble and in another way while reading the user data, it does not indicate that such reconfiguration occurs "before the discrete time sequence detector finishes processing the discrete time sample values of a current sector," as required by the claim.

For the foregoing reasons, the rejection of claim 43 and its dependent claims 44 and 52-56 based on Dudley is reversed. For the same reasons, so too is the rejection of independent method claim 57, which similarly recites "reconfiguring the timing recovery circuit and the gain control circuit before the sequence detector finishes processing the discrete time sample values of a current sector so that the read channel can begin acquiring an acquisition preamble of a next sector, thereby reducing a physical gap between sectors on the magnetic disk medium," and its dependent claims 58-63.

Turning now to Figure 2 of Petersen, Appellants do not deny that the claimed timing recovery circuit reads on data synchronizer 67, that the claimed gain control circuit reads on automatic gain control circuit 51, and that the claimed sequence detector reads on pulse detector 63 in combination with encoder and decoder 73 (Answer at 3). We note that control signal SGT (Figure 3(B)) causes each of automatic gain control circuit 51, filter system 55, and pulse detector 63 to be configured in one way during servo burst intervals (signal portion 143 in Figure 3(A)), while control signal RGT causes each of those circuits to be configured in another way during data intervals (signal portions 141 and 154 in Figure 3(A)). Id. at col. 6, ll. 11-24 and 42-66; col. 9, ll. 14-31 and 58-64. However,

presumably because these control signals are not described as changing state part way through a data interval, the examiner does not argue that the effect of these controls signals is to reconfigure the timing recovery circuit and the gain control circuit before the discrete time sequence detector finishes processing the discrete time sample values of a current sector, as required by the claim. Instead, the examiner contends that "Figures 1 and 2 of Petersen show controller 25 and control logic 85 controlling automatic gain control circuit 51, filter 55, pulse detector 63, and data synchronizer 67 in a continuous, concurrent, parallel, and, thus, a pipeline mode. See column 5, lines 45-67, et seq. of Petersen." Answer at 5. The cited passage in Petersen begins by stating that "[t]he controller 25 constantly monitors and commands operation of the circuit chip 29 [which includes the circuits in question] over the control bus 47." The examiner's argument is unconvincing because the "continuous, concurrent, [and] parallel" operations to which he refers are the functions performed by the circuits in question during the servo burst and data intervals and thus do not constitute reconfiguration of the timing recovery and gain control circuits in the sense of claims 43 and 57, i.e., changing the operating parameters of those circuits.

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As a result, the rejection of independent claims 43 and 57 and dependent claims 44-54 and 58-61 for anticipation by Petersen is also reversed.

REVERSED

JOHN C. MARTIN)	
Administrative Patent Judge)	
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)	
JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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