

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JASON CHEN, BAO-SHIANG SUN, and HENRY FAN

Appeal No. 2000-1251
Application No. 08/843,786

ON BRIEF

Before FLEMING, LALL, and LEVY, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge.***

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 12-13 and 20-22. Claims 1-6, 8-11 and 14-15 are not part of the appeal.¹

The invention relates to an integrated circuit (IC) and a method for protecting an IC against the consequences of having erroneously entered a test mode during normal operation. The IC (1) includes a start test mode circuit for generating a test mode

¹ Claims 1-6 and 8-11 have been indicated as allowable in Paper No. 8. Claims 14-15 have been objected to in Paper No. 8 as being dependent upon a rejected claim, but would be allowable if rewritten in independent form incorporating the limitations of claims 12-13.

start-up signal (TEST) to cause the IC to enter a test mode and a reset circuit (220) coupled to the start test mode circuit and responsive to the test mode start-up signal (TEST) for resetting the IC after the IC has erroneously entered a test mode during normal operation. See Appellants' specification on page 7, lines 20-30, page 9, lines 20-24 and associated figures 1-2. The method includes the steps of generating the test mode start-up signal (TEST) during normal operation of the IC (1) and resetting the IC (1) based on receipt of the test mode start-up signal (TEST). See Appellants' specification on page 7, lines 23-30, page 9, lines 5-24 and associated figures 1-2.

Independent claims 12 and 20 present in the application are reproduced as follows:

12. An integrated circuit, comprising:

a start test mode circuit for generating a test mode start-up signal to cause the integrated circuit to enter a test mode; and

a reset circuit coupled to the start test mode circuit and responsive to the test mode start-up signal for resetting the integrated circuit after the integrated circuit has erroneously entered a test mode during normal operation.

20. A method for protecting an integrated circuit against the consequences of having erroneously entering [sic; entered] a test mode during normal operation, in which the integrated circuit comprises a start test mode circuit for generating a test mode start-up signal to cause the integrated circuit to enter a test mode, wherein the method comprises the steps of:

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(a) generating a test mode start-up signal during normal operation of the integrated circuit; and

(b) resetting the integrated circuit based on the receipt of the test mode start-up signal.

References

The references relied upon by the Examiner are as follows:

Miyawaki et al. (Miyawaki)	4,970,727	Nov. 13, 1990
Slemmer et al. (Slemmer)	5,072,138	Dec. 10, 1991
McClure	5,493,532	Feb. 20, 1996

Rejections at Issue

Claims 12 and 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Slemmer in view of Miyawaki. Claims 13, 21, and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Slemmer in view of Miyawaki and McClure.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief² and the Answer for the respective details thereof.

² Appellants filed an appeal brief on September 10, 1999, Paper No. 10. The Examiner responded in an Examiner's Answer, Paper No. 13, mailed November 6, 2001.

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OPINION

With full consideration being given the subject matter on appeal, the Examiner's rejections and the arguments of Appellants and Examiner, for the reasons stated *infra*, we reverse the Examiner's rejections of claims 12-13 and 20-22 under 35 U.S.C. § 103.

We first will address the rejection of claims 12 and 20 under 35 U.S.C. § 103 as being unpatentable over Slemmer in view of Miyawaki. The Examiner states that Slemmer includes a start test mode circuit and a reset circuit (40,60). Examiner's Answer, Page 3, lines 14-16. The Examiner acknowledges that Slemmer does not discuss a reset circuit responsive to the test mode start-up signal for resetting the IC as recited in claim 12. Examiner's Answer, Page 3, lines 17-18. To provide a motivation for having the reset circuit of Slemmer responsive to a test mode start-up signal for resetting the IC, the Examiner cites Miyawaki. The Examiner argues that Miyawaki teaches various special modes for test evaluation known in the semiconductor memory art, including a reset memory mode which responds to a high voltage detection or test start-up signal. Examiner's Answer, Page 3, lines 18-20. The Examiner then concludes that it

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would have been obvious to one of ordinary skill in the art to make the reset circuit of Slemmer responsive to a test mode start-up signal, such as the reset signal used in the reset memory mode taught by Miyawaki, since resetting an IC is desirable or necessary once the special mode function has been completed. See Examiner's Answer, Page 4, lines 1-4.

Appellants argue that Slemmer does not disclose a reset circuit responsive to the test mode start-up signal for resetting the integrated circuit after the integrated circuit has erroneously entered a test mode during normal operation. See Appeal Brief, Page 4, lines 29-31. Rather, Appellants state that Slemmer "focuses its efforts on preventing the IC from erroneously entering the test mode to begin with." Appeal Brief, Page 6, lines 36-37. Additionally, Appellants argue that Miyawaki does not teach the use of a test mode start-up signal to reset an IC after the IC has erroneously entered a test mode during normal operations. Appeal Brief, Page 8, lines 1-4. Thus, Appellant states that the combination of Slemmer with Miyawaki does not provide the claimed invention. Appeal Brief, Page 8, line 36 through Page 9, line 6.

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of

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obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ 1443, 1444 (Fed Cir. 1992). See also **In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 87 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all the evidence and arguments." **In re Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. [T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). With these principles in mind, we commence review of the pertinent evidence and arguments of Appellants and Examiner.

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Upon careful review, we fail to find that the Examiner has provided the requisite findings in Slemmer or Miyawaki of a reset circuit responsive to a test mode start-up signal for resetting the IC after the IC has erroneously entered a test mode during normal operation as recited in claim 12 or the step of resetting the IC based on receipt of the test mode start-up signal as recited in claim 20. As Appellant correctly points out, the reset circuit (40,46) of Slemmer completely locks out the test mode during power-up of memory. See Abstract, column 10, lines 23-26, and column 12, lines 62-65 of Slemmer. This reset circuit is thus not responsive to the test mode start-up signal and does not reset the IC based upon receipt of the signal. Rather, the reset circuit locks out or prevents entry of test mode signals during power-up of the device.

With respect to Miyawaki, Miyawaki does teach a test mode that involves resetting the memory. This test mode involves sending a signal to reset the memory. However, this signal was not erroneously entered during normal operation as recited by claim 12. Rather, the signal to reset the memory as taught by Miyawaki was correctly entered or desired during memory operation. Thus, Miyawaki does not teach the limitation of a reset circuit responsive to the test mode start-up signal for

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resetting the integrated circuit *after the integrated circuit has erroneously entered a test mode during normal operation* as recited in claim 12. In addition, the discussions in Miyawaki also do not teach a method for protecting an IC *against the consequences of having erroneously entered a test mode during normal operation* comprising the step of resetting the IC based on the receipt of the test mode start-up signal as recited in claim 20.

We note that columns 31-32 of Slemmer recognizes the problem of an IC erroneously entering a test mode during normal operation. This discussion in Slemmer centers on either a complete shutdown of the system or using a chip enabling function to deal with the consequences of the IC inadvertently entering test mode during normal operation. In the complete shutdown method, Slemmer is silent regarding whether the shutdown is accomplished using a reset circuit responsive to a test mode start-up signal, and we refuse to speculate. In the chip enabling function method, Slemmer discloses in column 33, lines 6-9 that the possibility of entering test mode inadvertently during normal operation is eliminated. Thus, upon review of columns 31-32 of Slemmer, we find these methods do not provide a teaching to include a reset circuit responsive to a test mode

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start-up signal as recited in claim 12 or resetting the IC based on the receipt of the test mode start-up signal as recited in claim 20.

We therefore fail to find that Slemmer or Miyawaki disclose or teach "a reset circuit responsive to the test mode start-up signal for resetting the integrated circuit after the integrated circuit has erroneously entered a test mode during normal operation" as recited in claim 12 or a method "for protecting an integrated circuit against the consequences of having erroneously entered a test mode during normal operation . . . , wherein the method comprises the steps of: (a) generating a test mode start-up signal during normal operation of the integrated circuit; and (b) resetting the integrated circuit based on the receipt of the test mode start-up signal" as recited in claim 20. As such, we cannot sustain the rejection of claims 12 and 20 as being obvious over Slemmer in view of Miyawaki.

We now turn to the rejection of claims 13 and 21-22 under 35 U.S.C. § 103 as being unpatentable over Slemmer in view of Miyawaki and McClure. The Examiner has not relied on the McClure reference to teach or suggest a reset circuit responsive to the test mode start-up signal for resetting the IC after the IC has erroneously entered a test mode during normal operation as

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recited in claim 12 or the steps of the method for protecting an IC against the consequences of having erroneously entered a test mode during normal operation of generating a test mode start-up signal during normal operation of the IC and resetting the IC based on the receipt of the test mode start-up signal as recited in claim 20. As such, we also cannot sustain the rejections of claims 13 and 21-22 made under 35 U.S.C. § 103.

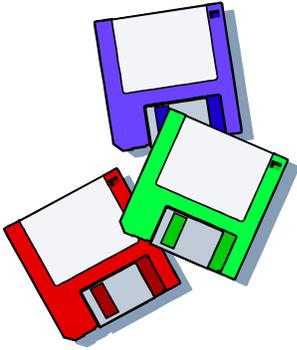
REVERSED

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DECISION: REVERSED

Prepared: June 19, 2003

Draft Final

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PALM / ACTS 2 / BOOK

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