

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD H. ST. PIERRE JR. and EDWIN W. RESLER

Appeal No. 2000-0671
Application No. 08/909,507

ON BRIEF

Before HAIRSTON, KRASS and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-15, all of the pending claims.

The invention is directed to an interface board for receiving modular interface cards and finds utility in the field of boundary scan interfaces in accordance with the IEEE 1149.1 standard developed by the Joint Test Action Group (JTAG).

Representative independent claim 1 is reproduced as follows:

1. A system for implementing a boundary scan chain, said system comprising:

an interface board comprising:

a connector for transferring boundary scan signals; and

a plurality of interfaces coupled in series in a predetermined order, and in parallel to receive a plurality of said boundary scan signals;

and at least one card comprising:

a socket for receiving an integrated circuit; and

a connector interface, coupled to said socket, for removably coupling with one of said plurality of interfaces.

The examiner relies on the following references:

Jarwala et al. [Jarwala] 5,331,274 Jul. 19, 1994

Chang et al. [Chang] 5,544,309 Aug. 06, 1996

Claims 1-3, 9 and 15 stand rejected under 35 U.S.C. § 102 (b) as anticipated by Jarwala.

Claims 4-8 and 10-14 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner offers Jarwala with regard to claims 4 and 5, adding Chang with regard to claims 6-8 and 10-14.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

With regard to the rejection under 35 U.S.C. § 102 (b), the examiner cites

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column 2, lines 1-33, column 5, lines 13-20, and Figure 3 of Jarwala as disclosure of a technique for testing at least one I/O connection of a circuit board simultaneously with the testing of at least one device on the board which contains at least one first boundary scan register, noting that Jarwala further teaches a serial test extension module (STEM) which physically mates with the pins of an edge connector on the circuit board through which the I/O connections to the board are made. Thus, according to the examiner, Jarwala teaches an interface board 30 comprising a connector, and a plurality of interfaces on a STEM 28 with a plurality of separate sockets 32-32k for mating with edge connector 18 on a circuit board 10 so that a connector and a plurality of interfaces coupled in series and in parallel receive a plurality of boundary scan signals.

The examiner further cites column 5, lines 31-33, of Jarwala for devices 12-12n being mounted on a board 10 with connector interface 18; and he cites column 5, lines 20-24, for an edge connector 18 on a circuit board 10 to allow different types of circuit boards to be mated with STEM 28'. The examiner concludes that Jarwala thus teaches at least one card comprising a socket and being removably coupled with one of a plurality of interfaces.

Appellants argue, at page 6 of the brief, that Jarwala does not disclose a device which can be used to program ISP devices and that Jarwala "pertains to only one 'card'

or circuit board 10.” Such arguments are not persuasive since they pertain to limitations not appearing in the claims. For example, independent claim 1 recites nothing about programming an ISP device and the claim calls for “at least one card,” which includes only one card, which appellants apparently admit is disclosed by Jarwala.

However, we will not sustain the rejection of claims 1-3, 9 and 15 under 35 U.S.C. § 102 (b) because we agree with other arguments made by appellants. Independent claim 1 requires, inter alia, a socket for receiving an integrated circuit and a connector interface, coupled to the socket, for removably coupling with one of the plurality of interfaces.

It is the examiner’s position that the claimed sockets correspond to Jarwala’s sockets 32-32k. However, these sockets connect Jarwala’s circuit board 10 to STEM body 30. The examiner calls Jarwala’s STEM body 30 an interface board, which is accurate enough. Thus, the examiner is equating Jarwala’s STEM body 30 to the claimed “connector interface” and Jarwala’s circuit board 10 to the claimed “integrated circuit.” Under such an interpretation, it can, indeed, be said that Jarwala discloses a socket 32 for receiving an integrated circuit 10 but where is the “connector interface,” as claimed, which is “coupled to the socket, for removably coupling with one of said plurality of interfaces”? If Jarwala’s body 30 is the “connector interface,” and it might be

reasonably said that the body 30 is “coupled to the socket” 32, then Jarwala does not removably couple body 30 to one of the plurality of interfaces. This is so because if Jarwala’s circuit board 10 corresponds to the claimed “integrated circuit” which is part of “at least one card,” and STEM body 30 corresponds to the claimed “interface board,” then body 30 must have a “plurality of interfaces coupled in series in a predetermined order, and in parallel to receive a plurality of said boundary scan signals.” If this “plurality of interfaces” is constituted by Jarwala’s boundary scan registers 36, then it is unclear how a “connector interface” is “removably coupling with one of said plurality of interfaces” in Jarwala.

In response to appellants’ argument about Jarwala not disclosing that either the card 10 or the modules 31 includes a socket for receiving an integrated circuit 12 and that the sockets 32, contacts 34" and modules 31 do not receive any ICs, especially ICs 12, since the sockets receive card 10, which is not an IC (plus the fact that sockets 32, contacts 34" and modules 31 are not on the card 10 but on the body 30), the examiner states that “such sockets would clearly be included since Jarwala teaches (col. 3, lines 2-8) that the devices 12-12n are themselves configured as boundary scan devices and also includes non-boundary devices thus Jarwala supports both types of

devices and thus would include sockets to be able to switch between a boundary scan device and a non-boundary scan device” [answer-page 8].

Thus, it appears that the examiner's position has shifted from the rejection rationale set forth in the statement of the rejection to the examiner's response to appellants' arguments, and it is no longer clear what the examiner considers, in Jarwala, as corresponding elements to the instant claimed subject matter. If the examiner is now, somehow, attributing an inherency to Jarwala regarding the claimed sockets, we disagree since it is not necessarily so that Jarwala provides sockets in order to switch boundary scan and non-boundary scan devices, as the examiner implies. Such devices may very well be soldered to the board and not removably coupled thereto. We simply do not know, as Jarwala does not show any sockets connecting these devices to circuit board 10. Even if it might have been obvious to so connect such devices, the rejection before us is one of anticipation under 35 U.S.C. § 102 and not one of obviousness under 35 U.S.C. § 103.

Since the examiner has not shown that each and every claimed element and its functional relationship with the other claimed elements is taught by Jarwala, we will not sustain the rejection of claims 1-3, 9 and 15 under 35 U.S.C. § 102 (b).

We also will not sustain the rejection of claims 4 and 5 under 35 U.S.C. § 103, as unpatentable over Jarwala because while the examiner argues that it would have been obvious to provide a cascade input connector and a cascade output connector in Jarwala, the problem, outlined supra, with regard to the corresponding elements and

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the sockets, still exists.

Similarly, we will not sustain the rejection of claims 6-8 and 10-14 under 35 U.S.C. § 103 over Jarwala in view of Chang because Chang does not provide for the deficiencies of Jarwala, noted supra with regard to the rejection under 35 U.S.C. § 102(b).

The examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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