

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIH-CHIANG YU

Appeal No. 95-2861
Application 08/062,237¹

ON BRIEF

Before THOMAS, HAIRSTON, and CARMICHAEL, Administrative Patent
Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed May 17, 1993.

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This is an appeal from the final rejection of claims 4 through 7. In an Amendment After Final (paper number 10), claim 4 was amended.

The disclosed invention relates to a non-volatile semiconductor memory device.

Claim 4 is illustrative of the claimed invention, and it reads as follows:

4. A non-volatile semiconductor memory device comprising:
 - a semiconductor substrate;
 - a source and a drain formed in said semiconductor substrate, said source spaced from said drain;
 - a channel disposed between said source and said drain;
 - a pair of first control gates dielectrically disposed atop portions of said channel;
 - a second control gate dielectrically disposed atop said pair of first control gates and substantially perpendicular therewith; and
 - a floating gate having end segments thereof dielectrically disposed between said pair of first control gates and said second control gate, and a mid segment thereof dielectrically disposed atop another portion of said channel;

wherein when said first and second control gates are substantially simultaneously energized to a first set of potential values, electrical charges are couplingly induced in said floating gate from said channel, allowing said floating gate to couplingly vary the conductivity of said channel after the de-energization of said control gate [sic, gates], and wherein when said first and second control gates are substantially simultaneously energized to a second set of potential values, electrical charges are couplingly induced out of said floating

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gate to said channel, allowing said floating gate to coupling [sic, couplingly] vary the conductivity of the channel after the de-energization of said control gates.

The references relied on by the examiner are:

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| Masuoka | 4,910,565 | Mar. 20, 1990 |
| Toshikazu (Japanese patent) (PTO Translation attached) | 58-54668 | Mar. 31, 1983 |

Muller et al. (Muller), "MOS Field-Effect Transistors I: Basic Theories and Models," Device Electronics for Integrated Circuits, pages 452 through 454 (2d ed., New York, John Wiley & Sons, 1986).

Claims 4 through 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Toshikazu in view of Masuoka.

Claims 4 through 7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Toshikazu in view of Masuoka and Muller.

Reference is made to the brief and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejections of claims 4 through 7.

We agree with the examiner's observation (Answer, page 3) that Toshikazu "teaches in Figure 2 a non-volatile semiconductor memory device having floating gate 25, a pair of first lower control gates 30 and 31 laterally surrounding the floating gate and an upper control gate 27 formed above." The examiner acknowledges (Answer, page 3) that "Toshikazu differs from the present invention in that the upper control gate 27 runs in the same direction as the pair of first lower control gates 30 and 31."

With this difference in mind, the examiner states (Answer, pages 3 and 4) that:

Masuoka teaches however in Figures 2-3 that the upper level control gate 114a may run orthogonal to lower gates 108a, 108b, and 106. It is noted that Masuoka teaches 108a, and 108b to be lateral floating gates surrounding control gate 106. This design is slightly different than that of Toshikazu which has two control gates laterally surrounding a floating gate. It would have been obvious to a skilled artisan to combine the teaching of Masuoka which shows the upper gate formed orthogonal to the lower gate layers in order to achieve integration of the device and conserve as much wafer space as possible.

Appellant argues (Brief, pages 6 and 7) that:

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To begin with, as conceded by the Examiner . . . the base cell of Masuoka is different from that of Toshikazu. In Masuoka, the floating gates 108a and 108b are disposed laterally surrounding the control gate 106 (Fig. 3 of Masuoka). In Toshikazu [sic, Toshikazu], the control gates 30 and 31 are disposed laterally surrounding the floating gate 25 (Fig. 2 of Toshikazu [sic, Toshikazu]). In addition, the Examiner points out that the control gates 114a and 106 of Masuoka are orthogonally disposed. Notwithstanding the Examiner's allegation, combining this feature of having the control gates orthogonally disposed, with the base cell of Toshikazu, as suggested by the Examiner, would still not satisfy the criteria as set forth in independent claims 4 and 7.

We agree. Appellant correctly argues (Brief, page 7) that Toshikazu modified by Masuoka would have the top control gate 27 "disposed atop only the floating gate 25, and not atop the pair of control gates 30 and 31." Moreover, the appellant correctly argues on the same page of the Brief that the combined reference teachings would not "include the end segments of floating gate 25 disposed between the pair of control gates 30 and 31 and the top control gate 27," and "would involve significant modifications and would also be deemed improper." In view of these differences between the teachings of the applied references and the claimed invention, we also agree with the appellant's arguments (Brief, pages 7 through 9) that the programming and erasure of the claimed device differs from the programming and erasure of the vastly different devices in the applied references. Accordingly,

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the obviousness rejection of claims 4 through 7 based upon the combined teachings of Toshikazu and Masuoka is reversed.

In the other obviousness rejection of claims 4 through 7, Muller is cited by the examiner (Answer, page 4) because it "teaches several programming and erase schemes for floating gate memory devices." On the same page of the Answer, the examiner concludes that it would have been obvious to a skilled artisan to combine the teachings of Muller with those of Toshikazu and Masuoka "in order to know how to program and erase the device." In view of the noted structural differences between the claimed device and the devices in Toshikazu and Masuoka, and the fact that Muller is merely cited for its programming and erasure teachings, this obviousness rejection of claims 4 through 7 is likewise reversed.

DECISION

The decision of the examiner rejecting claims 4 through 7 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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