EUROPEAN PATENT OFFICE
U.S. PATENT AND TRADEMARK OFFICE

CPC NOTICE OF CHANGES 516

MAY 1, 2018

PROJECT RP0375

The following classification changes will be effected by this Notice of Changes:

Action	**Subclass**	**Group(s)**
SCHEME:		
Titles Changed:	G11C	5/04
	G11C	7/10
	G11C	7/16
	G11C	7/22
	G11C	8/04
	G11C	11/06014
	G11C	11/35
	G11C	11/401
	G11C	11/4072
	G11C	11/409
	G11C	11/4093
	G11C	11/4096
	G11C	11/416
	G11C	11/419
	G11C	13/0002
	G11C	14/0018
	G11C	16/0466
	G11C	17/02
	G11C	19/282
	G11C	29/10
DEFINITIONS:		
Definitions New:	G11C	8/04
Definitions Modified:	G11C	7/10
	G11C	11/401
	G11C	11/4093

No other subclasses/groups are impacted by this Notice of Changes.

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This Notice of Changes includes the following *[Check the ones included]:*

1. CLASSIFICATION SCHEME CHANGES
   - ☒ A. New, Modified or Deleted Group(s)
   - ☐ B. New, Modified or Deleted Warning(s)
   - ☐ C. New, Modified or Deleted Note(s)
   - ☐ D. New, Modified or Deleted Guidance Heading(s)
2. DEFINITIONS
   - ☒ A. New or Modified Definitions (Full definition template)
   - ☒ B. Modified or Deleted Definitions (Definitions Quick Fix)
3. ☐ REVISION CONCORDANCE LIST (RCL)
4. ☐ CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)
5. ☐ CHANGES TO THE CROSS-REFERENCE LIST (CRL)

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1. CLASSIFICATION SCHEME CHANGES

A. New, Modified or Deleted Group(s)

SUBCLASS G11C - STATIC STORES

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C5/04	2	Supports for storage elements{, e.g. memory modules}; Mounting or fixing of storage elements on such supports	
M	G11C7/10	1	Input/output [I/O] data interface arrangements, e.g. I/O data control circuits, I/O data buffers	
M	G11C7/16	1	Storage of analogue signals in digital stores using an arrangement comprising analogue/digital [A/D] converters, digital memories and digital/analogue [D/A] converters	
M	G11C7/22	1	Read-write [R-W] timing or clocking circuits; Read-write [R-W] control signal generators or management	
M	G11C8/04	1	using a sequential addressing device, e.g. shift register, counter (using first in first out [FIFO] registers for changing speed of digital data flow G06F 5/06; using last in first out [LIFO] registers for processing digital data by operating upon their order G06F 7/00)	
M	G11C11/06014	4	{using one such element per bit}	
M	G11C11/35	3	with charge storage in a depletion layer, e.g. charge coupled devices {(in shift registers G11C 19/282)}	
M	G11C11/401	4	forming cells needing refreshing or charge regeneration, i.e. dynamic cells	
M	G11C11/4072	7	Circuits for initialisation, powering up or down, clearing memory or presetting	
M	G11C11/409	7	Read-write [R-W] circuits	
M	G11C11/4093	8	Input/output [I/O] data interface arrangements, e.g. data buffers	
M	G11C11/4096	8	Input/output [I/O] data management or control circuits, e.g. reading or writing circuits, I/O drivers or bit-line switches	
M	G11C11/416	7	Read-write [R-W] circuits	
M	G11C11/419	7	Read-write [R-W] circuits	
M	G11C13/0002	1	{using resistive RAM [RRAM] elements}	
M	G11C 14/0018	2	{whereby the nonvolatile element is an EEPROM element, e.g. a floating gate or metal-nitride-oxide-silicon [MNOS] transistor}	

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Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C 16/0466	3	{comprising cells with charge storage in an insulating layer, e.g. metal-nitride-oxide-silicon [MNOS], silicon-oxide-nitride-oxide-silicon [SONOS] (G11C 16/0483, G11C 16/0491 take precedence)}	
M	G11C 17/02	1	using magnetic or inductive elements (G11C 17/14 takes precedence)	
M	G11C19/282	2	{with charge storage in a depletion layer, i.e. charge coupled devices [CCD]}	
M	G11C 29/10	3	Test algorithms, e.g. memory scan [MScan] algorithms; Test patterns, e.g. checkerboard patterns	

*N = new entries where reclassification into entries is involved; C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; E= existing entries with enlarged file scope, which receive documents from C or D entries, e.g. when a limiting reference is removed from the entry title; M = entries with no change to the file scope (no reclassification); D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed; U = entries that are unchanged.

NOTES:

- **No {curly brackets} are used for titles in CPC only subclasses, e.g. C12Y, A23Y; 2000 series symbol titles of groups found at the end of schemes (orthogonal codes); or the Y section titles. The {curly brackets} are used for 2000 series symbol titles found interspersed throughout the main trunk schemes (breakdown codes).
- For U groups, the minimum requirement is to include the U group located immediately prior to the N group or N group array, in order to show the N group hierarchy and improve the readability and understanding of the scheme. Always include the symbol, indent level and title of the U group in the table above.
- All entry types should be included in the scheme changes table above for better understanding of the overall scheme change picture. Symbol, indent level, and title are required for all types except "D" which requires only a symbol.
- #"Transferred to" column must be completed for all C, D, F, and Q type entries. F groups will be deleted once reclassification is completed.
- When multiple symbols are included in the "Transferred to" column, avoid using ranges of symbols in order to be as precise as possible.
- For administrative transfer of documents, the following text should be used: "< administrative transfer to XX>" or "<administrative transfer to XX and YY simultaneously>" when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be "invention information", unless otherwise indicated, and to 2000 series groups is assumed to be "additional information".

2. A. DEFINITIONS (new)

Insert the following new definition.

G11C 8/04

References

Limiting references

This place does not cover:

Using first in first out [FIFO] registers for changing speed of digital data flow	G06F 5/06
Using last in first out [LIFO] registers for processing digital data by operating upon their order	G06F 7/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Addressing within memory systems with multidimensional access, e.g. row/column, matrix	G06F 12/0207

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2. B. DEFINITIONS QUICK FIX

Symbol	**Location of change** (e.g., section title)	**Existing reference symbol or text**	**Action; New symbol; New text**
G11C 7/10			Insert a new *Informative references* section and the following row: References Informative references *Attention is drawn to the following places, which may be of interest for search*: Level conversion circuits in general H03K 19/0175
G11C 7/10	Limiting references	Level conversion circuits in general H03K 19/0175	Delete the entire *Limiting references* section and table.
G11C 11/401			Insert a new *Informative references* section and table and the following three rows: References Informative references *Attention is drawn to the following places, which may be of interest for search*: Ferro-electric RAMs or FeRAMs G11C11/22 The much less frequent refreshing or updating of data in non-volatile memories G11C 16/3418, G11C 13/0021 Fabrication, integration, layout of DRAM cells H01L 27/108
G11C 11/401	Limiting references	Ferro-electric RAMs or FeRAMs G11C11/22 The much less frequent refreshing or updating of data in non-volatile memories G11C 16/3418, G11C 13/0021 Fabrication, integration, layout of DRAM cells H01L 27/108	Delete the entire *Limiting references* section and table.
G11C 11/4093	Informative references		Insert the following row into to the *Informative references* table: Level conversion circuits in general H03K 19/0175
G11C 11/4093	Limiting references	Level conversion circuits in general H03K 19/0175	Delete the entire *Limiting references* section.

NOTES:

- The table above is used for corrections or modifications to existing definitions, e.g. delete an entire definition or part thereof; propose new wording or modify wording of a section, change the symbol the definition is associated with, change or delete a reference symbol, etc.
- Do not delete (F) symbol definitions.