EUROPEAN PATENT OFFICE
U.S. PATENT AND TRADEMARK OFFICE

CPC NOTICE OF CHANGES 343

DATE: JANUARY 1, 2017

PROJECT RP0400

The following classification changes will be effected by this Notice of Changes:

Action	**Subclass**	**Group(s)**
Title wording changes:	G11C	subclass
	H01L	21/77, 27/00, 27/0211, 27/0222, 27/0225, 27/0233, 27/0248, 27/0255, 27/1023, 27/1025, 27/108, 27/10802, 27/1085, 27/10873, 27/11, 27/115, 27/11502, 27/11504, 27/11507, 27/11509, 27/11512, 27/11514, 27/11517, 27/11519, 27/11521, 27/11524, 27/11526, 27/11529, 27/11531, 27/11534, 27/11536, 27/11539, 27/11541, 27/11543, 27/11546, 27/11548, 27/11551, 27/11553, 27/11556, 27/11558, 27/1156, 27/11563, 27/11565, 27/11568, 27/1157, 27/11573, 27/11575, 27/11578, 27/1158, 27/11582, 27/11585, 27/11587, 27/1159, 27/11592, 27/11595, 27/11597, 27/1274, 27/13
Scheme warning to be modified:	H01L	Subclass
Scheme note to be modified:	H01L	27/00
Modified definitions:	H01L	27/108, 27/13

No other subclasses/groups are impacted by this Notice of Changes.

This Notice of Changes includes the following *[Check the ones included]:*

1. CLASSIFICATION SCHEME CHANGES
   - ☒ A. New, Modified or Deleted Group(s)
   - ☒ B. New, Modified or Deleted Warning Notice(s)
   - ☒ C. New, Modified or Deleted Note(s)
   - ☐ D. New, Modified or Deleted Guidance Heading(s)
2. DEFINITIONS (New or Modified)
   - ☒ A. DEFINITIONS (Full definition template)

☐ B. DEFINITIONS (Definitions Quick Fix)

3. ☐ REVISION CONCORDANCE LIST (RCL)

4. ☒ CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)

5. ☐ CROSS-REFERENCE LIST (CRL)

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1. CLASSIFICATION SCHEME CHANGES

A. Modified Group(s)

SUBCLASS G11C – STATIC STORES

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	G11C	Subclass	STATIC STORES (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L27/108-H01L27/11597; pulse technique in general H03K, e.g. electronic switches H03K17/00)	

SUBCLASS H01L – SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	H01L21/77	2	Manufacture or treatment of devices consisting of a plurality of solid state components or integrated circuits formed in, or on, a common substrate (electrically programmable read-only memories or multistep manufacturing processes therefor H01L27/115)	
M	H01L27/00	0	Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate (details thereof H01L23/00, H01L29/00-H01L51/00; assemblies consisting of a plurality of individual solid state devices H01L25/00)	
M	H01L27/0211	4	{adapted for requirements of temperature}	
M	H01L27/0222	5	{Charge pumping, substrate bias generation structures}	
M	H01L27/0225	5	{Charge injection in static induction transistor logic structures [SITL]}	
M	H01L27/0233	5	{Integrated injection logic structures [I2L]}	
M	H01L27/0248	3	{for electrical or thermal protection, e.g. electrostatic discharge [ESD] protection}	
M	H01L27/0255	5	{using diodes as protective elements}	
M	H01L27/1023	6	{Bipolar dynamic random access memory structures}	
M	H01L27/1025	6	{Static bipolar memory cell structures}	

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	H01L27/108	5	Dynamic random access memory structures	
M	H01L27/10802	6	{comprising floating-body transistors, e.g. floating-body cells}	
M	H01L27/1085	8	{with at least one step of making the capacitor or connections thereto}	
M	H01L27/10873	8	{with at least one step of making the transistor}	
M	H01L27/11	5	Static random access memory structures	
M	H01L27/115	6	Electrically programmable read-only memories; Multistep manufacturing processes therefor	
M	H01L27/11502	7	with ferroelectric memory capacitors	
M	H01L27/11504	8	characterised by the top-view layout	
M	H01L27/11507	8	characterised by the memory core region	
M	H01L27/11509	8	characterised by the peripheral circuit region	
M	H01L27/11512	8	characterised by the boundary region between the core and peripheral circuit regions	
M	H01L27/11514	8	characterised by the three-dimensional arrangements, e.g. with cells on different height levels	
M	H01L27/11517	7	with floating gate	
M	H01L27/11519	8	characterised by the top-view layout	
M	H01L27/11521	8	characterised by the memory core region (three-dimensional arrangements H01L27/11551)	
M	H01L27/11524	9	with cell select transistors, e.g. NAND	
M	H01L27/11526	8	characterised by the peripheral circuit region	
M	H01L27/11529	9	of memory regions comprising cell select transistors, e.g. NAND	
M	H01L27/11531	9	Simultaneous manufacturing of periphery and memory cells	
M	H01L27/11534	10	including only one type of peripheral transistor	
M	H01L27/11536	11	with a control gate layer also being used as part of the peripheral transistor	
M	H01L27/11539	11	with an inter-gate dielectric layer also being used as part of the peripheral transistor	
M	H01L27/11541	11	with a floating-gate layer also being used as part of the peripheral transistor	
M	H01L27/11543	11	with a tunnel dielectric layer also being used as part of the peripheral transistor	
M	H01L27/11546	10	including different types of peripheral transistor	
M	H01L27/11548	8	characterised by the boundary region between the core and peripheral circuit regions	
M	H01L27/11551	8	characterised by three-dimensional arrangements, e.g. with cells on different height levels	
M	H01L27/11553	9	with source and drain on different levels, e.g. with sloping channels	
M	H01L27/11556	10	the channels comprising vertical portions, e.g. U-shaped channels	

Type*	**Symbol**	**Indent Level Number of dots (e.g. 0, 1, 2)**	**Title (new or modified) "CPC only" text should normally be enclosed in {curly brackets}****	**Transferred to#**
M	H01L27/11558	8	the control gate being a doped region, e.g. single-poly memory cells	
M	H01L27/1156	8	the floating gate being an electrode shared by two or more components	
M	H01L27/11563	7	with charge-trapping gate insulators, e.g. MNOS or NROM	
M	H01L27/11565	8	characterised by the top-view layout	
M	H01L27/11568	8	characterised by the memory core region (three-dimensional arrangements H01L27/11578)	
M	H01L27/1157	9	with cell select transistors, e.g. NAND	
M	H01L27/11573	8	characterised by the peripheral circuit region	
M	H01L27/11575	8	characterised by the boundary region between the core and peripheral circuit regions	
M	H01L27/11578	8	characterised by three-dimensional arrangements, e.g. with cells on different height levels	
M	H01L27/1158	9	with source and drain on different levels, e.g. with sloping channels	
M	H01L27/11582	10	the channels comprising vertical portions, e.g. U-shaped channels	
M	H01L27/11585	7	with the gate electrodes comprising a layer used for its ferroelectric memory properties, e.g. metal-ferroelectric-semiconductor [MFS] or metal-ferroelectric-metal-insulator-semiconductor [MFMIS]	
M	H01L27/11587	8	characterised by the top-view layout	
M	H01L27/1159	8	characterised by the memory core region	
M	H01L27/11592	8	characterised by the peripheral circuit region	
M	H01L27/11595	8	characterised by the boundary region between core and peripheral circuit regions	
M	H01L27/11597	8	characterised by three-dimensional arrangements, e.g. cells on different height levels	
M	H01L27/1274	6	{using crystallisation of amorphous semiconductor or recrystallisation of crystalline semiconductor}	
M	H01L27/13	3	combined with thin-film or thick-film passive components	

*N = new entries where reclassification into entries is involved; C = entries with modified file scope where reclassification of documents from the entries is involved; Q = new entries which are firstly populated with documents via administrative transfers from deleted (D) entries. Afterwards, the transferred documents into the Q entry will either stay or be moved to more appropriate entries, as determined by intellectual reclassification; E= existing entries with enlarged file scope, which receive documents from C or D entries, e.g. when a limiting reference is removed from the entry title; M = entries with no change to the file scope (no reclassification); D = deleted entries; F = frozen entries will be deleted once reclassification of documents from the entries is completed; U = entries that are unchanged.

NOTES:

- **No {curly brackets} are used for titles in CPC only subclasses, e.g. C12Y, A23Y; 2000 series symbol titles of groups found at the end of schemes (orthogonal codes); or the Y section titles. The {curly brackets} are used for 2000 series symbol titles found interspersed throughout the main trunk schemes (breakdown codes).

- For U groups, the minimum requirement is to include the U group located immediately prior to the N group or N group array, in order to show the N group hierarchy and improve the readability and understanding of the scheme. Always include the symbol, indent level and title of the U group in the table above.
- All entry types should be included in the scheme changes table above for better understanding of the overall scheme change picture. Symbol, indent level, and title are required for all types except "D" which requires only a symbol.
- #"Transferred to" column must be completed for all C, D, F, and Q type entries. F groups will be deleted once reclassification is completed.
- When multiple symbols are included in the "Transferred to" column, avoid using ranges of symbols in order to be as precise as possible.
- For administrative transfer of documents, the following text should be used: "< administrative transfer to XX>" or "<administrative transfer to XX and YY simultaneously>" when administrative transfer of the same documents is to more than one place.
- Administrative transfer to main trunk groups is assumed to be "invention information", unless otherwise indicated, and to 2000 series groups is assumed to be "additional information".

B. New, Modified or Deleted Warning notice(s)

SUBCLASS H01L – SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR

Type*	**Location**	**Old Warning notice**	**New/Modified Warning notice**
D	SUBCLASS	H01L21/8239 covered by H01L27/1052	
D	SUBCLASS	H01L21/8247 covered by H01L27/11517	

*N = new warning, M = modified warning, D = deleted warning

NOTE: The “Location” column only requires the symbol PRIOR to the location of the warning. No further directions such as “before” or “after” are required.

C. Modified Note

SUBCLASS H01L – SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR

Type*	**Location**	**Old Note**	**New/Modified Note**
M	H01L27/00	In this group, in the absence of an indication to the contrary, classification is made in the last appropriate place.	1. In this group, with the exception of groups H01L27/115 - H01L27/11597, the last place priority rule is applied, i.e. at each hierarchical level, in the absence of an indication to the contrary, classification is made in the last appropriate place. 2. When classifying in this group, subject matter relating to electrically programmable read-only memories is classified in group H01L27/115, irrespective of the last place priority rule.

*N = new note, M = modified note, D = deleted note

NOTE: The “Location” column only requires the symbol PRIOR to the location of the note. No further directions such as “before” or “after” are required.

2. A. DEFINITIONS (modified)

H01L27/108

References

Delete: Limiting references section

Insert: second row of Informative references, “Bipolar DRAMs…” as shown below:

Informative references

Attention is drawn to the following places, which may be of interest for search:

Circuits	G11C11/24, G11C11/401
Bipolar DRAMs	H01L27/1023

H01L27/13

References

Delete: Limiting references section

Replace with: New Informative references section, as shown below (Row 3 is **new text** and the other three rows to be re-arranged in proper sequence):

Informative references

Attention is drawn to the following places, which may be of interest for search:

Storage capacitors associated with the pixel electrode in AMLCD displays	G02F1/136213
RFID circuits	G06K19/07749

Memories employing capacitors, e.g. DRAM passive two-terminal components without a potential-jump or surface barrier for integrated circuits, details thereof and multistep manufacturing processes therefor	H01L27/108
SOI arrangements	H01L27/12

4. CHANGES TO THE CPC-TO-IPC CONCORDANCE LIST (CICL)

CPC	**IPC**	**Action***
H01L27/11502	H01L27/11502	update
H01L27/11504	H01L27/11504	update
H01L27/11507	H01L27/11507	update
H01L27/11509	H01L27/11509	update
H01L27/11512	H01L27/11512	update
H01L27/11514	H01L27/11514	update
H01L27/11517	H01L27/11517	update
H01L27/11519	H01L27/11519	update
H01L27/11521	H01L27/11521	update
H01L27/11524	H01L27/11524	update
H01L27/11526	H01L27/11526	update
H01L27/11529	H01L27/11529	update
H01L27/11531	H01L27/11531	update
H01L27/11534	H01L27/11534	update
H01L27/11536	H01L27/11536	update
H01L27/11539	H01L27/11539	update
H01L27/11541	H01L27/11541	update
H01L27/11543	H01L27/11543	update
H01L27/11546	H01L27/11546	update
H01L27/11548	H01L27/11548	update
H01L27/11551	H01L27/11551	update
H01L27/11553	H01L27/11553	update
H01L27/11556	H01L27/11556	update
H01L27/11558	H01L27/11558	update
H01L27/1156	H01L27/1156	update
H01L27/11563	H01L27/11563	update
H01L27/11565	H01L27/11565	update
H01L27/11568	H01L27/11568	update
H01L27/1157	H01L27/1157	update
H01L27/11573	H01L27/11573	update
H01L27/11575	H01L27/11575	update
H01L27/11578	H01L27/11578	update
H01L27/1158	H01L27/1158	update
H01L27/11582	H01L27/11582	update
H01L27/11585	H01L27/11585	update
H01L27/11587	H01L27/11587	update
H01L27/1159	H01L27/1159	update
H01L27/11592	H01L27/11592	update
H01L27/11595	H01L27/11595	update
H01L27/11597	H01L27/11597	update

*Action column:

- For an (N) or (Q) entry, provide an IPC symbol and complete the Action column with “NEW.”
- For an existing CPC main trunk entry or indexing entry where the existing IPC symbol needs to be changed, provide an updated IPC symbol and complete the Action column with “UPDATED.”

- For a (D) CPC entry or indexing entry complete the Action column with “DELETE.” IPC symbol does not need to be included in the IPC column.
- For an (N) 2000 series CPC entry which is positioned within the main trunk scheme (breakdown code) provide an IPC symbol and complete the action column with “NEW”.
- For an (N) 2000 series CPC entry positioned at the end of the CPC scheme (orthogonal code), with no IPC equivalent, complete the IPC column with “CPCONLY” and complete the action column with “NEW”.

NOTES:

- F symbols are not included in the CICL table above.
- E and M symbols are not included in the CICL table above unless a change to the existing IPC is desired.