U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

CLASSIFICATION ORDER 1897

OCTOBER 5, 2010

PROJECT E-6978

The following classification changes will be effected by this order:

	Class	**Subclass**	**Art Unit**	**Ex'r Search Room**
Abolished:	716	1-21	2825	OS0001
Established:	716	30, 50-56, 100-139	2825	OS0001
Title Change:	716		2825	OS0001

The following classes are also impacted by this order:

257, 326, 327, 340, 359, 361, 505, 700, 703, 704, 707, 708, 709, 712, 713, 714, 717

This order includes the following:

A. CLASSIFICATION MANUAL CHANGES

B. LISTING OF PRINCIPAL SOURCE OF ESTABLISHED AND DISPOSITION OF ABOLISHED SUBCLASSES

C. CHANGES TO THE USPC-TO-IPC CONCORDANCE

D. DEFINITION CHANGES AND NEW OR ADDITIONAL DEFINITIONS

CLASSIFICATION ORDER 1897

OCTOBER 5, 2010

PROJECT E-6978

Project Leader:	Yen M. Nguyen
Project Classifier:	Nam T. Nguyen
Examiner:	Stacy Whitmore
Editor:	David Delzingaro
Publications Specialist:	Louise Bogans

30 **NANOTECHNOLOGY RELATED INTEGRATED CIRCUIT DESIGN**
50 **DESIGN OF SEMICONDUCTOR MASK OR RETICLE**
51 .Analysis and verification (process flow, inspection)
52 ..Defect (including design rule checking)
53 ..Optical proximity correction (including RET)
54 .Manufacturing optimizations
55 .Layout generation (polygon, pattern feature)
56 .Yield
100 **INTEGRATED CIRCUIT DESIGN PROCESSING**
101 .Logic design processing
102 ..Design entry
103 ..Translation (logic-to-logic, logic-to-netlist, netlist processing)
104 ..Logic circuit synthesis (mapping logic)
105 ...With partitioning
106 ..Design verification (functional simulation, model checking)
107 ...Equivalence checking
108 ...Timing verification (timing analysis)
109 ...Power estimation
110 .Physical design processing
111 ..Verification
112 ...Defect Analysis
113 ...Timing Analysis
114 ....Buffer or repeater insertion
115 ...Noise (e.g., crosstalk, electromigration, etc.)
116 ..Mapping circuit design to programmable logic devices (PLDs)
117 ...Configuring PLDs (including data file, bitstream generation, etc.)
118 ..Floorplanning
119 ...Placement or layout
120 ....Power distribution
121 ....For PLDs
122 ....Constraint-based
123 ....Iteration
124 ....With partitioning
125 ...With partitioning
126 ..Routing
127 ...Power (voltage islands)
128 ...PLDs
129 ...Global
130 ...Detailed
131 ...With partitioning
132 .Optimization
133 ..For power
134 ..For timing
135 ..For area
136 .Testing or Evaluating
137 .PCB, MCM Design
138 .System-on-chip design
139 .Layout editor (with ECO, reuse, GUI)

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

FOR 100 **CIRCUIT DESIGN (716/1)**
FOR 101 .Optimization (e.g., redundancy, compaction) (716/2)
FOR 102 .Translation (e.g., conversion, equivalence) (716/3)
FOR 103 .Testing or evaluating (716/4)
FOR 104 ..Design verification (e.g., wiring line capacitance, fanout checking, minimum path width) (716/5)
FOR 105 ...Timing analysis (e.g., delay time, path delay, latch timing) (716/6)
FOR 106 .Partitioning (e.g., function block, ordering constraint) (716/7)
FOR 107 .Floorplanning (716/8)
FOR 108 ..Detailed placement (i.e., iterative improvement) (716/9)

FOR 109 ..Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance) (716/10)
FOR 110 ..Layout editor (e.g., updating) (716/11)
FOR 111 .Routing (e.g., routing map, netlisting) (716/12)
FOR 112 ..Global routing (e.g., shortest path, dead space, or duplicate trace elimination) (716/13)
FOR 113 ..Detailed routing (e.g., channel routing, switch box routing((716/14)
FOR 114 ..PCB wiring (716/15)
FOR 115 ..PLA, PLD, FPGA, OR MCM (716/16)
FOR 116 .Programmable integrated circuit (e.g., basic cell, standard cell, macrocell) (716/17)
FOR 117 .Logical circuit synthesizer (716/18)
FOR 118 **DESIGN OF SEMICONDUCTOR MASK (716/19)**
FOR 119 .Mesh generation (716/20)
FOR 120 .Pattern exposure (716/21)

APPLICATIONS (364/400)

FOR 489 .Circuit design and analysis (364/489)
FOR 490 ..Integrated (364/490)
FOR 491 ...Layout (364/491)

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
118/715	1	716/4	1120
174/250	2	716/1	693
174/257	1	716/19	518
	1	716/5	867
174/258	1	716/6	827
174/260	1	716/15	126
174/261	1	716/15	126
228/104	1	716/19	518
228/4.5	1	716/19	518
250/214 R	1	716/6	827
250/307	1	716/20	73
250/310	2	716/21	397
250/396 R	3	716/21	397
250/398	2	716/21	397
250/400	1	716/21	397
250/492.2	4	716/21	397
250/492.21	1	716/21	397
250/492.22	2	716/21	397
250/559.04	1	716/4	1120
257/202	1	716/8	324
257/203	1	716/1	693
	1	716/10	470
	1	716/12	421
	1	716/19	518
	1	716/2	571
	1	716/4	1120
	2	716/16	387
	3	716/17	267
	3	716/8	324
257/204	1	716/1	693
	1	716/17	267
257/206	1	716/14	114
	1	716/16	387
	2	716/10	470
	2	716/8	324
257/207	1	716/10	470
	1	716/14	114
	1	716/2	571
	2	716/13	214
	2	716/17	267
	3	716/1	693
	3	716/12	421

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	4	716/8	324
257/208	1	716/12	421
	1	716/16	387
	1	716/17	267
	1	716/19	518
	1	716/8	324
257/210	1	716/13	214
	1	716/17	267
257/211	1	716/12	421
257/212	1	716/4	1120
257/288	1	716/19	518
257/355	1	716/1	693
	2	716/7	188
257/356	1	716/2	571
257/360	1	716/10	470
	1	716/17	267
257/369	1	716/17	267
	1	716/4	1120
257/374	1	716/1	693
257/390	1	716/21	397
257/391	1	716/4	1120
257/439	1	716/10	470
257/467	1	716/19	518
257/48	1	716/17	267
	1	716/19	518
	1	716/5	867
	3	716/4	1120
257/499	1	716/1	693
257/506	1	716/1	693
257/508	1	716/12	421
257/522	1	716/5	867
257/529	1	716/12	421
257/531	1	716/1	693
257/532	1	716/12	421
	2	716/1	693
257/618	1	716/21	397
257/659	1	716/21	397
	2	716/12	421
257/665	1	716/12	421
257/666	1	716/1	693
	1	716/11	334
257/685	1	716/1	693

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
257/690	1	716/1	693
	1	716/15	126
257/695	1	716/12	421
257/700	1	716/9	187
257/723	1	716/16	387
257/730	1	716/1	693
257/734	1	716/10	470
	1	716/4	1120
257/737	1	716/15	126
257/751	1	716/13	214
257/754	1	716/10	470
257/758	1	716/14	114
	1	716/9	187
257/762	1	716/1	693
257/773	1	716/10	470
	1	716/11	334
	1	716/12	421
	1	716/13	214
	1	716/21	397
	1	716/9	187
	3	716/1	693
	3	716/8	324
257/774	1	716/10	470
	1	716/14	114
	1	716/2	571
	3	716/13	214
257/775	1	716/13	214
257/776	1	716/12	421
	1	716/16	387
257/786	1	716/10	470
	1	716/11	334
	1	716/13	214
257/787	1	716/8	324
29/825	1	716/4	1120
29/846	1	716/19	518
29/847	1	716/19	518
307/64	1	716/17	267
323/234	1	716/8	324
323/271	1	716/1	693
323/313	1	716/3	275
323/316	1	716/1	693
323/354	1	716/1	693

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
324/207.15	1	716/1	693
324/501	1	716/6	827
	2	716/4	1120
324/519	1	716/4	1120
324/520	1	716/4	1120
324/522	1	716/5	867
324/548	1	716/5	867
324/613	1	716/16	387
324/658	1	716/4	1120
324/66	2	716/4	1120
324/678	1	716/4	1120
324/73.1	1	716/4	1120
324/750.15	2	716/4	1120
324/750.22	1	716/4	1120
324/750.3	1	716/4	1120
324/755.01	2	716/19	518
	3	716/4	1120
324/76.19	1	716/4	1120
324/762.01	3	716/4	1120
324/762.02	1	716/4	1120
324/762.03	2	716/4	1120
324/762.05	1	716/4	1120
324/762.06	1	716/12	421
	1	716/2	571
	2	716/4	1120
324/762.09	1	716/4	1120
	1	716/5	867
324/763.01	1	716/1	693
	2	716/4	1120
324/764.01	2	716/4	1120
326/101	1	716/1	693
	1	716/12	421
	1	716/16	387
	1	716/17	267
	2	716/8	324
326/103	2	716/19	518
	3	716/2	571
326/107	1	716/19	518
326/11	1	716/16	387
326/113	1	716/3	275
	1	716/8	324
326/121	1	716/10	470

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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
326/16	1	716/16	387
326/21	1	716/17	267
326/28	1	716/17	267
326/30	1	716/1	693
	1	716/17	267
	1	716/2	571
326/34	1	716/10	470
326/37	1	716/1	693
	1	716/11	334
	1	716/17	267
	5	716/16	387
326/38	1	716/11	334
	1	716/15	126
	1	716/19	518
	1	716/3	275
	2	716/2	571
	2	716/6	827
	3	716/8	324
	4	716/1	693
	4	716/4	1120
	5	716/12	421
	21	716/17	267
	30	716/16	387
326/39	1	716/1	693
	2	716/17	267
	6	716/16	387
326/40	1	716/2	571
	1	716/3	275
	1	716/6	827
	2	716/16	387
	2	716/17	267
326/41	1	716/14	114
	1	716/18	478
	1	716/19	518
	1	716/2	571
	1	716/21	397
	1	716/3	275
	5	716/17	267
	8	716/12	421
	19	716/16	387
326/44	1	716/19	518
326/45	1	716/17	267

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New Classification	Number of ORs	Source Classification	Number of ORs
326/46	1	716/5	867
326/49	1	716/8	324
326/8	1	716/17	267
	1	716/8	324
326/80	1	716/10	470
	1	716/4	1120
326/81	1	716/1	693
	1	716/13	214
326/82	1	716/8	324
326/83	1	716/1	693
326/87	1	716/1	693
326/93	2	716/1	693
	2	716/6	827
326/94	1	716/6	827
326/96	1	716/13	214
	1	716/6	827
326/97	1	716/10	470
327/119	1	716/1	693
327/129	1	716/8	324
327/141	1	716/10	470
	1	716/12	421
	1	716/6	827
327/144	2	716/6	827
327/147	1	716/6	827
327/149	1	716/1	693
	1	716/6	827
327/152	1	716/1	693
327/156	1	716/14	114
327/158	1	716/1	693
327/267	1	716/4	1120
327/276	1	716/1	693
327/277	1	716/6	827
327/285	1	716/6	827
327/291	1	716/13	214
327/292	1	716/6	827
327/295	2	716/6	827
327/312	1	716/6	827
327/33	1	716/1	693
327/334	1	716/10	470
327/382	1	716/6	827
327/512	1	716/4	1120
327/530	1	716/1	693

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New Classification	Number of ORs	Source Classification	Number of ORs
327/536	1	716/17	267
327/554	1	716/12	421
330/250	1	716/4	1120
331/2	1	716/4	1120
333/12	1	716/1	693
333/124	1	716/1	693
333/128	1	716/15	126
333/142	1	716/6	827
333/185	1	716/5	867
333/24 R	1	716/1	693
333/246	1	716/5	867
333/4	1	716/15	126
	1	716/17	267
338/308	1	716/8	324
341/80	1	716/1	693
347/262	1	716/21	397
348/87	1	716/4	1120
355/67	1	716/21	397
356/237.5	1	716/5	867
356/394	1	716/5	867
356/401	1	716/8	324
356/509	1	716/21	397
360/46	1	716/8	324
361/56	1	716/10	470
361/679.31	1	716/15	126
361/679.32	1	716/1	693
361/720	1	716/15	126
361/748	1	716/15	126
365/151	1	716/9	187
365/158	1	716/16	387
365/185.19	1	716/16	387
365/185.2	1	716/14	114
	1	716/17	267
365/185.22	1	716/5	867
365/185.23	1	716/1	693
365/185.27	1	716/1	693
365/189.011	1	716/1	693
365/189.05	1	716/13	214
	2	716/1	693
365/189.07	1	716/1	693
365/189.11	1	716/1	693
365/201	1	716/1	693

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New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/4	1120
365/226	1	716/1	693
365/227	1	716/1	693
365/230.04	1	716/21	397
365/51	1	716/1	693
365/63	1	716/1	693
	1	716/10	470
	1	716/13	214
	1	716/8	324
374/121	1	716/1	693
375/233	1	716/4	1120
382/141	1	716/21	397
382/144	1	716/21	397
	1	716/4	1120
	3	716/19	518
382/145	1	716/4	1120
382/149	1	716/11	334
	1	716/4	1120
	1	716/7	188
382/150	1	716/4	1120
382/151	2	716/4	1120
382/278	1	716/4	1120
414/222.13	1	716/19	518
430/22	1	716/19	518
	4	716/21	397
430/296	2	716/19	518
430/30	2	716/20	73
	4	716/19	518
	5	716/21	397
430/311	2	716/21	397
430/322	1	716/19	518
430/5	1	716/4	1120
	1	716/9	187
	12	716/21	397
	18	716/19	518
438/10	1	716/4	1120
	1	716/5	867
	1	716/6	827
438/12	1	716/4	1120
438/127	1	716/1	693
438/128	1	716/1	693
	1	716/10	470

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New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/19	518
438/129	1	716/14	114
	1	716/16	387
	1	716/19	518
	1	716/2	571
	1	716/7	188
	2	716/1	693
	2	716/17	267
	2	716/3	275
438/14	1	716/21	397
438/15	1	716/10	470
	1	716/17	267
	1	716/21	397
	1	716/3	275
	2	716/19	518
	2	716/4	1120
438/16	1	716/21	397
	1	716/5	867
438/164	1	716/12	421
438/17	1	716/1	693
	1	716/2	571
	1	716/4	1120
438/18	2	716/19	518
	7	716/4	1120
438/275	1	716/19	518
438/30	1	716/10	470
438/306	1	716/5	867
438/382	1	716/11	334
438/385	1	716/1	693
438/401	1	716/21	397
438/5	1	716/5	867
438/510	1	716/20	73
438/599	1	716/1	693
	1	716/16	387
438/622	1	716/8	324
438/626	1	716/1	693
438/692	1	716/7	188
438/7	2	716/4	1120
438/703	1	716/21	397
438/94	1	716/21	397
439/75	1	716/8	324
600/322	1	716/19	518

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New Classification	Number of ORs	Source Classification	Number of ORs
700/104	1	716/3	275
	1	716/5	867
700/108	1	716/1	693
	1	716/19	518
	1	716/5	867
700/109	1	716/4	1120
	2	716/19	518
700/110	1	716/1	693
	1	716/10	470
	1	716/19	518
	1	716/21	397
	2	716/4	1120
700/111	1	716/19	518
700/121	1	716/10	470
	1	716/11	334
	1	716/2	571
	2	716/1	693
	3	716/4	1120
	4	716/21	397
	6	716/19	518
700/29	1	716/2	571
700/95	1	716/19	518
700/96	1	716/14	114
700/97	1	716/20	73
700/99	1	716/2	571
702/118	1	716/4	1120
702/183	1	716/1	693
702/189	1	716/5	867
702/19	1	716/8	324
702/35	1	716/4	1120
702/59	1	716/4	1120
702/64	1	716/5	867
702/82	1	716/21	397
702/84	1	716/4	1120
702/94	1	716/4	1120
703/12	1	716/21	397
703/13	1	716/5	867
703/14	1	716/14	114
	1	716/5	867
	2	716/1	693
	3	716/4	1120
	4	716/20	73

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New Classification	Number of ORs	Source Classification	Number of ORs
703/15	1	716/4	1120
703/16	2	716/4	1120
703/19	1	716/1	693
703/2	1	716/12	421
	1	716/15	126
	1	716/19	518
	1	716/6	827
	1	716/9	187
	2	716/2	571
	3	716/5	867
	4	716/1	693
	9	716/4	1120
	19	716/20	73
703/21	1	716/4	1120
703/23	1	716/1	693
703/4	1	716/4	1120
703/5	1	716/2	571
703/7	1	716/4	1120
705/51	1	716/3	275
705/59	2	716/4	1120
706/13	2	716/16	387
706/20	1	716/4	1120
706/23	1	716/20	73
708/627	1	716/1	693
708/629	1	716/1	693
708/704	1	716/5	867
709/208	1	716/7	188
709/223	1	716/13	214
	1	716/18	478
	1	716/3	275
709/225	1	716/1	693
709/226	1	716/4	1120
710/10	1	716/1	693
710/313	1	716/1	693
710/38	1	716/12	421
710/8	1	716/14	114
	1	716/3	275
	1	716/8	324
711/104	1	716/1	693
	1	716/10	470
711/105	1	716/1	693
711/133	1	716/1	693

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New Classification	Number of ORs	Source Classification	Number of ORs
711/3	1	716/8	324
711/5	1	716/1	693
712/15	1	716/17	267
712/201	1	716/10	470
712/216	1	716/4	1120
712/23	1	716/8	324
	1	716/9	187
712/32	1	716/10	470
712/33	1	716/19	518
712/36	1	716/17	267
712/43	1	716/17	267
713/100	1	716/16	387
713/150	1	716/1	693
713/160	1	716/1	693
713/2	1	716/18	478
713/300	1	716/14	114
713/400	1	716/6	827
714/25	1	716/17	267
	1	716/4	1120
714/30	1	716/1	693
	1	716/16	387
	1	716/18	478
	5	716/4	1120
714/7	1	716/17	267
714/704	1	716/4	1120
714/724	4	716/4	1120
714/725	1	716/5	867
	3	716/4	1120
714/726	1	716/20	73
	1	716/6	827
	4	716/4	1120
714/727	1	716/1	693
	2	716/4	1120
714/729	1	716/4	1120
714/731	1	716/4	1120
714/732	2	716/4	1120
714/733	2	716/4	1120
714/734	3	716/4	1120
714/736	1	716/4	1120
	1	716/6	827
714/738	4	716/4	1120
714/739	1	716/1	693

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/4	1120
714/744	1	716/6	827
714/792	1	716/1	693
715/209	1	716/11	334
716/100	1	716/11	334
	1	716/12	421
	1	716/13	214
	1	716/14	114
	1	716/15	126
	1	716/16	387
	1	716/19	518
	1	716/3	275
	1	716/3	275
	1	716/4	1120
	1	716/5	867
	2	716/17	267
	2	716/17	267
	3	716/1	693
	8	716/4	1120
	9	716/10	470
	10	716/5	867
	10	716/6	827
	33	716/1	693
716/101	1	716/10	470
	1	716/11	334
	1	716/11	334
	1	716/12	421
	1	716/14	114
	1	716/2	571
	1	716/3	275
	1	716/3	275
	1	716/6	827
	2	716/15	126
	2	716/16	387
	2	716/18	478
	2	716/2	571
	2	716/7	188
	3	716/18	478
	3	716/4	1120
	3	716/4	1120
	4	716/17	267
	5	716/16	387

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	10	716/1	693
	16	716/1	693
716/102	1	716/12	421
	2	716/1	693
	2	716/13	214
	2	716/20	73
	2	716/7	188
	2	716/8	324
	4	716/19	518
	4	716/9	187
	5	716/17	267
	7	716/12	421
	7	716/15	126
	8	716/16	387
	10	716/18	478
	11	716/10	470
	16	716/17	267
	16	716/5	867
	17	716/3	275
	27	716/6	827
	32	716/4	1120
	33	716/2	571
	57	716/11	334
	67	716/18	478
	92	716/1	693
716/103	1	716/1	693
	1	716/17	267
	1	716/19	518
	1	716/19	518
	1	716/2	571
	1	716/4	1120
	1	716/8	324
	2	716/15	126
	3	716/10	470
	3	716/13	214
	3	716/3	275
	4	716/18	478
	4	716/9	187
	9	716/8	324
	11	716/7	188
	14	716/11	334
	15	716/17	267

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	16	716/16	387
	17	716/12	421
	39	716/6	827
	45	716/1	693
	47	716/2	571
	50	716/5	867
	63	716/4	1120
	118	716/18	478
	152	716/3	275
716/104	1	716/1	693
	1	716/15	126
	1	716/20	73
	1	716/21	397
	2	716/12	421
	2	716/17	267
	2	716/19	518
	2	716/7	188
	2	716/9	187
	3	716/13	214
	6	716/8	324
	7	716/12	421
	8	716/10	470
	10	716/11	334
	11	716/5	867
	13	716/16	387
	14	716/17	267
	17	716/4	1120
	22	716/3	275
	26	716/18	478
	29	716/6	827
	32	716/2	571
	43	716/1	693
	149	716/18	478
716/105	1	716/10	470
	1	716/12	421
	1	716/15	126
	1	716/16	387
	1	716/2	571
	1	716/4	1120
	1	716/8	324
	1	716/9	187
	2	716/4	1120

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	3	716/18	478
	3	716/7	188
	4	716/17	267
	4	716/3	275
	4	716/5	867
	6	716/1	693
	7	716/6	827
	9	716/2	571
	11	716/1	693
	19	716/7	188
	24	716/18	478
716/106	1	716/10	470
	1	716/12	421
	1	716/12	421
	1	716/13	214
	1	716/13	214
	1	716/15	126
	1	716/16	387
	1	716/19	518
	1	716/20	73
	1	716/20	73
	1	716/8	324
	2	716/17	267
	2	716/2	571
	2	716/4	1120
	3	716/1	693
	4	716/16	387
	6	716/11	334
	6	716/3	275
	7	716/18	478
	7	716/7	188
	8	716/18	478
	15	716/6	827
	18	716/2	571
	25	716/1	693
	153	716/4	1120
	228	716/5	867
716/107	1	716/10	470
	1	716/11	334
	1	716/12	421
	1	716/13	214
	1	716/16	387

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/16	387
	1	716/20	73
	1	716/6	827
	3	716/1	693
	3	716/1	693
	5	716/2	571
	6	716/7	188
	8	716/3	275
	14	716/4	1120
	41	716/5	867
716/108	1	716/11	334
	1	716/14	114
	1	716/16	387
	1	716/17	267
	2	716/12	421
	2	716/13	214
	2	716/18	478
	2	716/7	188
	2	716/9	187
	3	716/3	275
	4	716/10	470
	4	716/16	387
	6	716/17	267
	10	716/1	693
	23	716/2	571
	24	716/4	1120
	24	716/5	867
	188	716/6	827
716/109	1	716/1	693
	1	716/13	214
	1	716/14	114
	1	716/17	267
	1	716/19	518
	2	716/8	324
	3	716/18	478
	4	716/18	478
	4	716/6	827
	5	716/1	693
	11	716/2	571
	11	716/5	867
	17	716/4	1120
716/110	1	716/11	334

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/12	421
	1	716/14	114
	1	716/16	387
	1	716/16	387
	1	716/17	267
	1	716/2	571
	1	716/4	1120
	1	716/4	1120
	1	716/5	867
	1	716/6	827
	1	716/6	827
	1	716/7	188
	1	716/8	324
	4	716/1	693
	4	716/17	267
	7	716/1	693
716/111	1	716/1	693
	1	716/14	114
	1	716/16	387
	1	716/16	387
	1	716/17	267
	1	716/18	478
	1	716/18	478
	1	716/20	73
	1	716/4	1120
	1	716/6	827
	1	716/6	827
	1	716/8	324
	2	716/13	214
	2	716/15	126
	2	716/9	187
	3	716/10	470
	3	716/11	334
	3	716/17	267
	3	716/7	188
	5	716/12	421
	5	716/5	867
	11	716/1	693
	13	716/2	571
	21	716/5	867
	27	716/4	1120
716/112	1	716/13	214

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	2	716/14	114
	3	716/16	387
	3	716/19	518
	3	716/9	187
	4	716/3	275
	4	716/5	867
	6	716/17	267
	6	716/7	188
	7	716/6	827
	8	716/15	126
	8	716/8	324
	12	716/12	421
	14	716/2	571
	15	716/1	693
	15	716/13	214
	21	716/11	334
	25	716/10	470
	61	716/4	1120
	124	716/5	867
716/113	1	716/1	693
	1	716/13	214
	1	716/15	126
	1	716/17	267
	1	716/5	867
	4	716/17	267
	4	716/3	275
	5	716/14	114
	5	716/18	478
	8	716/7	188
	10	716/16	387
	10	716/9	187
	12	716/11	334
	12	716/6	827
	14	716/8	324
	19	716/13	214
	20	716/12	421
	25	716/1	693
	34	716/2	571
	38	716/5	867
	45	716/4	1120
	50	716/10	470
	331	716/6	827

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
716/114	1	716/16	387
	1	716/17	267
	1	716/18	478
	1	716/18	478
	1	716/3	275
	1	716/6	827
	2	716/17	267
	2	716/19	518
	2	716/7	188
	4	716/11	334
	4	716/4	1120
	5	716/14	114
	6	716/1	693
	6	716/5	867
	6	716/9	187
	9	716/13	214
	12	716/12	421
	12	716/8	324
	17	716/2	571
	40	716/10	470
	74	716/6	827
716/115	1	716/1	693
	1	716/16	387
	1	716/2	571
	1	716/21	397
	1	716/3	275
	1	716/6	827
	2	716/19	518
	2	716/9	187
	3	716/18	478
	3	716/7	188
	4	716/14	114
	4	716/8	324
	8	716/13	214
	10	716/11	334
	10	716/15	126
	14	716/10	470
	14	716/6	827
	15	716/12	421
	17	716/1	693
	23	716/2	571
	64	716/4	1120

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	124	716/5	867
716/116	1	716/1	693
	1	716/12	421
	1	716/3	275
	2	716/10	470
	2	716/4	1120
	3	716/16	387
	3	716/7	188
	3	716/8	324
	4	716/18	478
	4	716/2	571
	6	716/1	693
	14	716/17	267
	20	716/16	387
716/117	1	716/1	693
	1	716/14	114
	1	716/15	126
	2	716/16	387
	2	716/17	267
	2	716/19	518
	2	716/3	275
	2	716/6	827
	3	716/10	470
	3	716/18	478
	3	716/2	571
	4	716/11	334
	4	716/5	867
	4	716/7	188
	6	716/4	1120
	7	716/12	421
	10	716/1	693
	38	716/17	267
	84	716/16	387
716/118	1	716/14	114
	1	716/17	267
	1	716/19	518
	1	716/3	275
	1	716/9	187
	1	716/9	187
	2	716/13	214
	2	716/5	867
	4	716/1	693

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	4	716/10	470
	7	716/8	324
	8	716/8	324
	9	716/11	334
716/119	1	716/10	470
	1	716/13	214
	1	716/13	214
	1	716/15	126
	1	716/16	387
	1	716/19	518
	2	716/14	114
	2	716/16	387
	2	716/3	275
	2	716/6	827
	3	716/18	478
	3	716/4	1120
	3	716/5	867
	4	716/11	334
	4	716/17	267
	4	716/8	324
	5	716/7	188
	9	716/12	421
	14	716/2	571
	22	716/1	693
	22	716/9	187
	46	716/11	334
	47	716/10	470
	57	716/8	324
716/120	1	716/18	478
	1	716/19	518
	1	716/3	275
	1	716/8	324
	2	716/14	114
	2	716/15	126
	2	716/7	188
	4	716/2	571
	5	716/13	214
	5	716/5	867
	7	716/12	421
	7	716/9	187
	8	716/11	334
	11	716/1	693

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	16	716/8	324
	17	716/10	470
716/121	1	716/14	114
	1	716/4	1120
	1	716/8	324
	2	716/1	693
	2	716/2	571
	3	716/11	334
	3	716/12	421
	4	716/17	267
	4	716/7	188
	6	716/10	470
	6	716/17	267
	6	716/9	187
	9	716/16	387
	9	716/8	324
	13	716/16	387
716/122	1	716/18	478
	1	716/19	518
	1	716/6	827
	3	716/17	267
	3	716/5	867
	4	716/10	470
	4	716/14	114
	5	716/15	126
	6	716/1	693
	6	716/3	275
	7	716/13	214
	9	716/4	1120
	13	716/7	188
	15	716/12	421
	27	716/9	187
	31	716/11	334
	35	716/8	324
	38	716/2	571
	123	716/10	470
716/123	1	716/1	693
	1	716/13	214
	1	716/15	126
	1	716/17	267
	1	716/2	571
	1	716/6	827

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/9	187
	2	716/11	334
	2	716/13	214
	2	716/14	114
	2	716/16	387
	6	716/12	421
	10	716/7	188
	14	716/2	571
	17	716/10	470
	27	716/8	324
	52	716/9	187
716/124	1	716/14	114
	1	716/17	267
	1	716/19	518
	1	716/6	827
	2	716/1	693
	2	716/5	867
	3	716/12	421
	4	716/2	571
	6	716/10	470
	6	716/13	214
	7	716/9	187
	9	716/11	334
	13	716/8	324
	22	716/7	188
716/125	1	716/12	421
	1	716/16	387
	1	716/6	827
	1	716/7	188
	2	716/1	693
	2	716/17	267
	2	716/8	324
	3	716/12	421
	19	716/7	188
716/126	1	716/11	334
	1	716/17	267
	1	716/19	518
	1	716/20	73
	1	716/3	275
	1	716/4	1120
	1	716/6	827
	2	716/2	571

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	2	716/2	571
	2	716/8	324
	3	716/10	470
	3	716/11	334
	3	716/13	214
	3	716/14	114
	4	716/16	387
	5	716/13	214
	5	716/5	867
	13	716/1	693
	15	716/15	126
	26	716/12	421
	52	716/12	421
716/127	1	716/1	693
	1	716/13	214
	1	716/15	126
	1	716/16	387
	1	716/16	387
	1	716/17	267
	1	716/19	518
	1	716/2	571
	1	716/5	867
	1	716/6	827
	1	716/7	188
	1	716/8	324
	1	716/9	187
	2	716/10	470
	2	716/12	421
	3	716/14	114
	6	716/1	693
	7	716/12	421
	8	716/13	214
716/128	1	716/1	693
	1	716/10	470
	1	716/11	334
	1	716/13	214
	1	716/17	267
	1	716/2	571
	2	716/12	421
	3	716/14	114
	3	716/16	387
	8	716/12	421

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	20	716/16	387
716/129	1	716/1	693
	1	716/10	470
	1	716/14	114
	1	716/15	126
	1	716/18	478
	1	716/3	275
	1	716/5	867
	2	716/11	334
	2	716/16	387
	2	716/4	1120
	2	716/8	324
	3	716/15	126
	4	716/1	693
	4	716/12	421
	4	716/2	571
	7	716/7	188
	10	716/13	214
	17	716/14	114
	63	716/13	214
	65	716/12	421
716/130	1	716/17	267
	1	716/18	478
	1	716/19	518
	1	716/5	867
	1	716/6	827
	1	716/9	187
	2	716/1	693
	2	716/11	334
	2	716/12	421
	2	716/2	571
	3	716/13	214
	3	716/4	1120
	5	716/10	470
	6	716/14	114
	7	716/15	126
	30	716/12	421
	30	716/14	114
716/131	1	716/1	693
	1	716/10	470
	1	716/15	126
	1	716/8	324

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SOURCE CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	2	716/11	334
	3	716/7	188
	5	716/12	421
716/132	1	716/11	334
	1	716/15	126
	1	716/17	267
	1	716/18	478
	1	716/19	518
	1	716/6	827
	1	716/9	187
	2	716/19	518
	3	716/1	693
	3	716/13	214
	3	716/18	478
	3	716/4	1120
	3	716/5	867
	4	716/10	470
	4	716/2	571
	4	716/3	275
	7	716/4	1120
	8	716/1	693
	57	716/2	571
716/133	1	716/10	470
	1	716/15	126
	1	716/16	387
	1	716/2	571
	1	716/3	275
	1	716/4	1120
	2	716/18	478
	2	716/6	827
	7	716/1	693
	21	716/2	571
716/134	1	716/1	693
	1	716/1	693
	1	716/11	334
	1	716/12	421
	1	716/12	421
	1	716/13	214
	1	716/16	387
	1	716/2	571
	1	716/4	1120
	1	716/4	1120

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/7	188
	1	716/8	324
	2	716/18	478
	2	716/5	867
	9	716/6	827
	10	716/2	571
716/135	1	716/11	334
	1	716/15	126
	1	716/5	867
	1	716/8	324
	1	716/9	187
	2	716/1	693
	2	716/2	571
	2	716/4	1120
	2	716/6	827
	3	716/12	421
	13	716/2	571
716/136	1	716/10	470
	1	716/14	114
	1	716/16	387
	1	716/2	571
	1	716/20	73
	1	716/3	275
	1	716/9	187
	2	716/17	267
	2	716/2	571
	2	716/5	867
	3	716/19	518
	4	716/7	188
	5	716/6	827
	11	716/1	693
	20	716/5	867
	43	716/4	1120
	252	716/4	1120
716/137	1	716/17	267
	1	716/2	571
	1	716/3	275
	1	716/4	1120
	3	716/11	334
	3	716/17	267
	10	716/1	693
	12	716/15	126

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	23	716/15	126
716/138	1	716/11	334
	1	716/16	387
	1	716/19	518
	1	716/6	827
	1	716/8	324
	1	716/8	324
	2	716/4	1120
	3	716/17	267
	3	716/18	478
	3	716/4	1120
	4	716/5	867
	5	716/1	693
	10	716/17	267
	11	716/1	693
	53	716/16	387
716/139	1	716/13	214
	1	716/15	126
	1	716/16	387
	1	716/17	267
	1	716/17	267
	1	716/18	478
	1	716/19	518
	1	716/19	518
	1	716/20	73
	1	716/21	397
	1	716/3	275
	1	716/5	867
	2	716/10	470
	2	716/11	334
	2	716/2	571
	2	716/4	1120
	5	716/1	693
	17	716/11	334
716/30	1	716/1	693
	1	716/10	470
	1	716/12	421
	1	716/5	867
	2	716/1	693
	2	716/17	267
716/50	1	716/12	421
	1	716/13	214

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/15	126
	1	716/15	126
	1	716/16	387
	1	716/17	267
	1	716/18	478
	1	716/2	571
	1	716/20	73
	1	716/3	275
	1	716/4	1120
	1	716/7	188
	1	716/8	324
	2	716/1	693
	2	716/10	470
	2	716/16	387
	2	716/20	73
	2	716/5	867
	3	716/2	571
	4	716/1	693
	11	716/19	518
	20	716/21	397
	24	716/21	397
	35	716/19	518
716/51	1	716/1	693
	1	716/11	334
	1	716/12	421
	1	716/12	421
	1	716/4	1120
	1	716/7	188
	2	716/1	693
	2	716/10	470
	2	716/2	571
	2	716/5	867
	3	716/8	324
	6	716/20	73
	7	716/4	1120
	9	716/20	73
	18	716/19	518
	18	716/21	397
	21	716/19	518
	25	716/21	397
716/52	1	716/1	693
	1	716/17	267

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	1	716/6	827
	4	716/3	275
	5	716/10	470
	5	716/20	73
	7	716/21	397
	7	716/9	187
	9	716/8	324
	10	716/11	334
	12	716/2	571
	15	716/19	518
	35	716/4	1120
	37	716/5	867
	69	716/21	397
	87	716/19	518
716/53	1	716/1	693
	1	716/1	693
	1	716/11	334
	1	716/20	73
	2	716/20	73
	3	716/10	470
	3	716/5	867
	5	716/8	324
	8	716/2	571
	11	716/4	1120
	20	716/19	518
	28	716/21	397
	63	716/21	397
	104	716/19	518
716/54	1	716/10	470
	1	716/12	421
	1	716/14	114
	1	716/17	267
	1	716/18	478
	1	716/18	478
	1	716/20	73
	2	716/1	693
	2	716/10	470
	2	716/11	334
	2	716/3	275
	2	716/4	1120
	3	716/1	693
	3	716/4	1120

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	3	716/5	867
	3	716/9	187
	4	716/8	324
	9	716/21	397
	11	716/19	518
	13	716/2	571
	18	716/19	518
	20	716/21	397
716/55	1	716/13	214
	1	716/16	387
	1	716/2	571
	1	716/6	827
	2	716/1	693
	2	716/13	214
	2	716/17	267
	3	716/12	421
	3	716/18	478
	3	716/19	518
	4	716/3	275
	4	716/4	1120
	4	716/7	188
	5	716/10	470
	5	716/11	334
	5	716/9	187
	6	716/12	421
	6	716/20	73
	8	716/1	693
	10	716/11	334
	10	716/2	571
	11	716/5	867
	11	716/8	324
	42	716/21	397
	61	716/19	518
716/56	1	716/12	421
	1	716/12	421
	1	716/14	114
	1	716/2	571
	1	716/21	397
	1	716/5	867
	2	716/19	518
	5	716/19	518
	6	716/21	397

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SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by Data Control Division

New Classification	Number of ORs	Source Classification	Number of ORs
	21	716/4	1120

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/19	518	716/51	18
716/11	334	716/103	14
716/21	397	716/104	1
716/15	126	716/106	1
716/11	334	716/112	21
716/7	188	716/113	8
716/15	126	716/129	3
716/1	693	716/130	2
716/2	571	716/137	1
716/5	867	716/138	4
716/15	126	716/50	1
716/2	571	716/52	12
716/1	693	716/100	33
716/19	518	716/102	4
716/9	187	716/105	1
716/1	693	716/110	7
716/4	1120	716/113	45
716/9	187	716/114	6
716/17	267	716/114	2
716/18	478	716/122	1
716/2	571	716/123	14
716/16	387	716/127	1
716/5	867	716/132	3
716/6	827	716/133	2
716/15	126	716/137	12
716/11	334	716/137	3
716/18	478	716/55	3
716/10	470	716/100	9
716/2	571	716/101	2
716/1	693	716/113	25
716/18	478	716/115	3
716/1	693	716/131	1
716/17	267	716/136	2
716/3	275	716/54	2
716/8	324	716/102	2
716/6	827	716/105	7
716/2	571	716/116	4
716/11	334	716/119	46
716/2	571	716/128	1
716/4	1120	716/51	7
716/2	571	716/102	33
716/1	693	716/111	11
716/12	421	716/115	15

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/9	187	716/130	1
716/3	275	716/137	1
716/6	827	716/138	1
716/5	867	716/53	3
716/7	188	716/105	19
716/12	421	716/113	20
716/5	867	716/118	2
716/17	267	716/125	2
716/11	334	716/130	2
716/18	478	716/134	2
716/17	267	716/137	3
716/8	324	716/138	1
716/11	334	716/52	10
716/13	214	716/102	2
716/3	275	716/103	152
716/17	267	716/105	4
716/2	571	716/107	5
716/1	693	716/124	2
716/12	421	716/131	5
716/4	1120	716/138	3
716/11	334	716/54	2
716/19	518	716/56	5
716/16	387	716/103	16
716/19	518	716/104	2
716/10	470	716/111	3
716/7	188	716/112	6
716/6	827	716/113	331
716/8	324	716/113	14
716/15	126	716/126	15
716/14	114	716/56	1
716/12	421	716/127	2
716/1	693	716/117	1
716/16	387	716/139	1
716/12	421	716/130	2
716/19	518	716/54	11
716/18	478	716/109	4
716/13	214	716/132	3
716/5	867	716/100	1
716/9	187	716/123	1
716/10	470	716/136	1
716/7	188	716/105	3
716/13	214	716/113	1
716/16	387	716/125	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/13	214	716/129	10
716/16	387	716/106	1
716/17	267	716/110	4
716/2	571	716/136	1
716/21	397	250/492.21	1
716/19	518	228/104	1
716/5	867	365/185.22	1
716/19	518	703/2	1
716/4	1120	382/149	1
716/12	421	257/211	1
716/4	1120	382/151	2
716/6	827	327/149	1
716/5	867	438/306	1
716/12	421	257/203	1
716/14	114	710/8	1
716/21	397	250/400	1
716/12	421	710/38	1
716/5	867	714/725	1
		324/548	1
716/17	267	257/48	1
716/1	693	257/204	1
716/13	214	326/81	1
716/9	187	257/758	1
716/6	827	327/141	1
716/3	275	326/38	1
716/16	387	326/37	5
716/1	693	257/203	1
		438/127	1
716/6	827	327/144	2
716/19	518	430/5	18
716/8	324	257/202	1
716/16	387	438/599	1
716/2	571	257/356	1
716/1	693	708/629	1
716/17	267	326/30	1
716/4	1120	257/212	1
716/3	275	323/313	1
716/19	518	438/18	2
716/4	1120	365/201	1
716/20	73	706/23	1
716/4	1120	714/726	4
716/19	518	430/30	4
716/3	275	438/15	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/2	571	326/38	2
716/4	1120	257/48	3
716/1	693	365/226	1
716/3	275	438/129	2
716/1	693	324/207.15	1
716/17	267	326/38	21
716/4	1120	703/2	9
716/6	827	438/10	1
716/16	387	714/30	1
716/1	693	438/385	1
716/6	827	327/295	2
716/21	397	438/401	1
716/4	1120	382/145	1
716/8	324	257/787	1
716/12	421	327/141	1
716/4	1120	324/750.22	1
716/17	267	307/64	1
716/20	73	703/14	4
716/5	867	703/14	1
716/4	1120	700/110	2
716/6	827	327/312	1
716/1	693	257/532	2
716/4	1120	324/762.05	1
716/21	397	257/659	1
716/4	1120	257/203	1
716/1	693	714/739	1
716/4	1120	703/14	3
716/21	397	700/121	4
716/14	114	365/185.2	1
716/4	1120	438/18	7
716/10	470	326/121	1
716/21	397	257/618	1
716/17	267	438/15	1
716/5	867	356/394	1
716/4	1120	702/118	1
716/21	397	438/16	1
716/4	1120	438/7	2
716/13	214	365/63	1
716/1	693	714/727	1
716/21	397	430/311	2
716/10	470	716/108	4
716/19	518	716/130	1
716/8	324	716/50	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/11	334	716/55	5
716/4	1120	714/731	1
716/12	421	257/207	3
		716/56	1
716/18	478	716/101	2
		716/111	1
716/3	275	716/112	4
716/17	267	716/113	4
716/19	518	716/114	2
716/1	693	716/116	6
716/12	421	716/127	7
716/10	470	716/51	2
716/12	421	716/101	1
716/8	324	716/105	1
716/4	1120	716/107	14
716/11	334	716/111	3
716/16	387	716/117	84
716/5	867	716/117	4
716/15	126	716/119	1
716/1	693	716/121	2
716/4	1120	716/121	1
716/3	275	716/129	1
716/7	188	716/131	3
716/8	324	716/134	1
716/2	571	716/54	13
716/8	324	716/109	2
716/15	126	716/111	2
716/17	267	716/116	14
716/12	421	716/134	1
716/9	187	716/135	1
716/18	478	716/102	67
716/17	267	716/112	6
716/14	114	716/114	5
716/9	187	716/115	2
716/11	334	716/123	2
716/10	470	716/124	6
716/1	693	716/127	6
		716/54	3
716/7	188	716/102	2
716/10	470	716/103	3
716/8	324	716/104	6
716/2	571	716/109	11

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/3	275	716/113	4
		716/114	1
716/18	478	716/119	3
716/1	693	716/122	6
716/13	214	716/128	1
716/1	693	716/138	11
716/21	397	716/52	69
716/2	571	716/53	8
716/6	827	716/100	10
716/5	867	716/105	4
716/7	188	716/115	3
716/11	334	716/122	31
716/18	478	716/132	1
716/3	275	716/136	1
716/11	334	716/138	1
716/17	267	716/139	1
716/10	470	716/30	1
716/2	571	716/51	2
716/4	1120	716/53	11
716/6	827	716/101	1
716/11	334	716/104	10
716/6	827	716/108	188
716/16	387	716/110	1
716/13	214	716/111	2
716/5	867	716/112	124
716/10	470	716/113	50
716/12	421	716/114	12
716/10	470	716/119	47
716/6	827	716/124	1
716/17	267	716/128	1
716/11	334	716/139	17
716/2	571	716/139	2
716/5	867	716/52	37
716/18	478	716/54	1
716/6	827	716/55	1
716/12	421	716/105	1
716/11	334	716/114	4
716/7	188	716/119	5
716/14	114	716/120	2
716/5	867	716/122	3
		716/130	1
716/8	324	716/131	1
716/6	827	716/135	2

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/2	571	716/105	1
716/13	214	716/108	2
716/17	267	716/113	1
716/15	126	716/129	1
716/12	421	716/100	1
716/1	693	716/100	3
716/4	1120	716/103	1
716/6	827	716/115	1
716/2	571	716/123	1
716/19	518	716/50	35
716/2	571	716/101	1
716/16	387	716/136	1
		716/100	1
716/14	114	716/110	1
716/1	693	716/54	2
716/4	1120	716/54	2
716/8	324	716/121	1
716/12	421	716/55	6
716/17	267	716/101	4
716/12	421	716/128	2
716/15	126	716/132	1
716/17	267	716/102	5
716/10	470	716/119	1
716/2	571	716/50	1
716/1	693	716/132	3
716/17	267	326/41	5
716/4	1120	714/724	4
716/19	518	326/103	2
716/1	693	327/119	1
716/4	1120	703/4	1
716/8	324	338/308	1
716/10	470	326/34	1
716/1	693	438/129	2
		257/499	1
716/5	867	257/48	1
716/20	73	430/30	2
716/1	693	323/316	1
716/19	518	430/22	1
716/1	693	713/150	1
716/19	518	326/44	1
716/4	1120	324/73.1	1
		324/764.01	2
716/9	187	365/151	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/1	693	365/201	1
716/6	827	714/736	1
716/13	214	365/189.05	1
716/19	518	438/275	1
716/1	693	327/158	1
716/19	518	712/33	1
716/3	275	700/104	1
716/21	397	430/30	5
716/1	693	365/189.07	1
716/13	214	257/210	1
716/10	470	257/754	1
		257/786	1
716/12	421	703/2	1
716/6	827	714/744	1
716/19	518	430/322	1
716/10	470	257/360	1
716/17	267	257/207	2
716/6	827	713/400	1
716/21	397	356/509	1
716/16	387	257/723	1
716/4	1120	29/825	1
716/6	827	326/93	2
716/12	421	326/38	5
716/8	324	702/19	1
716/1	693	438/626	1
716/15	126	361/748	1
716/11	334	257/666	1
716/9	187	712/23	1
716/2	571	324/762.06	1
716/16	387	706/13	2
716/11	334	257/786	1
716/19	518	700/110	1
716/4	1120	703/7	1
716/6	827	324/501	1
716/4	1120	257/369	1
716/21	397	250/398	2
716/4	1120	714/733	2
		330/250	1
716/11	334	715/209	1
716/17	267	326/37	1
716/7	188	257/355	2
716/4	1120	714/30	5
716/13	214	257/786	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/15	126	174/261	1
716/2	571	703/2	2
716/3	275	716/133	1
716/19	518	716/136	3
716/10	470	716/53	3
716/9	187	716/132	1
716/4	1120	250/559.04	1
716/1	693	365/185.27	1
716/4	1120	324/762.03	2
716/18	478	713/2	1
716/10	470	326/80	1
716/18	478	326/41	1
716/21	397	716/54	9
716/15	126	716/103	2
716/18	478	716/105	24
716/7	188	716/106	7
716/19	518	716/120	1
716/17	267	716/123	1
716/14	114	716/126	3
716/10	470	716/128	1
716/7	188	716/136	4
716/11	334	716/100	1
716/9	187	716/102	4
716/11	334	716/118	9
716/9	187	716/120	7
716/12	421	716/125	3
716/2	571	716/130	2
716/6	827	716/130	1
716/10	470	716/133	1
		716/52	5
716/19	518	716/55	61
716/17	267	716/117	38
716/19	518	716/117	2
716/7	188	716/120	2
716/2	571	716/122	38
716/20	73	716/126	1
716/6	827	716/127	1
716/8	324	716/51	3
716/11	334	716/102	57
716/16	387	716/107	1
716/18	478	716/109	3
716/7	188	716/114	2
716/1	693	716/123	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/14	114	716/128	3
716/8	324	716/129	2
716/6	827	716/132	1
716/5	867	716/135	1
716/1	693	716/136	11
		716/50	4
		716/51	2
716/2	571	716/104	32
716/6	827	716/110	1
716/16	387	716/112	3
716/2	571	716/115	23
716/17	267	716/118	1
716/16	387	716/119	2
716/8	324	716/122	35
716/6	827	716/123	1
716/7	188	716/125	19
716/4	1120	716/132	7
716/5	867	716/139	1
716/18	478	716/139	1
716/9	187	716/52	7
716/8	324	716/54	4
		716/110	1
716/13	214	716/113	19
716/18	478	716/117	3
716/13	214	716/123	2
716/21	397	716/139	1
716/17	267	716/103	15
716/18	478	716/103	118
716/5	867	716/104	11
716/16	387	716/111	1
716/11	334	716/115	10
716/3	275	716/117	2
716/10	470	716/122	123
716/19	518	716/122	1
716/16	387	716/126	4
716/1	693	716/126	13
716/17	267	716/126	1
716/8	324	716/55	11
716/16	387	716/101	2
716/7	188	716/104	2
716/10	470	716/107	1
716/18	478	716/113	5
716/5	867	716/114	6

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/16	387	716/114	1
		716/115	1
716/4	1120	716/116	2
716/8	324	716/119	57
716/1	693	716/120	11
716/5	867	716/120	5
716/6	827	716/125	1
716/2	571	716/126	2
716/9	187	716/127	1
716/5	867	716/134	2
716/14	114	716/136	1
716/20	73	716/51	6
716/18	478	716/101	3
716/14	114	716/100	1
716/1	693	716/105	6
716/2	571	716/110	1
716/1	693	716/115	1
716/20	73	716/50	2
716/21	397	716/53	28
716/11	334	716/101	1
716/5	867	716/136	2
716/8	324	716/106	1
716/16	387	716/50	2
716/2	571	716/106	2
716/16	387	716/119	1
716/13	214	716/112	1
		716/123	1
716/2	571	716/134	1
716/13	214	716/50	1
716/20	73	716/54	1
716/10	470	716/54	1
716/15	126	716/101	2
716/19	518	716/126	1
716/17	267	716/138	10
716/4	1120	716/138	2
		716/137	1
716/19	518	228/4.5	1
		414/222.13	1
		430/296	2
716/4	1120	324/755.01	3
716/6	827	327/382	1
716/21	397	438/15	1
716/16	387	324/613	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/1	693	326/38	4
716/4	1120	382/144	1
716/11	334	326/37	1
716/1	693	711/5	1
716/4	1120	324/762.09	1
716/16	387	326/39	6
716/19	518	438/128	1
716/1	693	700/110	1
		709/225	1
716/13	214	257/751	1
716/6	827	250/214 R	1
716/16	387	713/100	1
716/1	693	323/354	1
		327/530	1
716/19	518	700/109	2
716/1	693	365/189.05	2
716/8	324	257/203	3
716/10	470	257/734	1
716/5	867	438/5	1
716/1	693	365/189.011	1
716/2	571	326/30	1
716/17	267	712/15	1
716/1	693	703/19	1
716/16	387	438/129	1
716/1	693	257/374	1
716/4	1120	375/233	1
716/19	518	700/111	1
716/5	867	703/2	3
716/9	187	257/773	1
716/6	827	174/258	1
716/1	693	257/762	1
716/19	518	257/467	1
716/1	693	711/105	1
716/9	187	703/2	1
716/17	267	712/36	1
		365/185.2	1
716/14	114	257/206	1
716/4	1120	118/715	1
716/10	470	365/63	1
716/1	693	365/189.11	1
716/20	73	700/97	1
716/19	518	257/208	1
716/17	267	326/39	2

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/10	470	257/773	1
716/14	114	326/41	1
716/21	397	326/41	1
716/7	188	716/116	3
716/12	421	716/104	7
716/13	214	716/120	5
716/14	114	716/108	1
716/18	478	716/138	3
716/19	518	326/41	1
716/4	1120	714/734	3
716/8	324	356/401	1
716/20	73	716/51	9
716/9	187	716/104	2
716/14	114	716/115	4
716/16	387	716/121	13
716/10	470	716/123	17
716/1	693	716/129	4
716/9	187	716/136	1
716/6	827	716/52	1
716/4	1120	716/55	4
716/13	214	716/55	1
716/16	387	716/102	8
716/1	693	716/105	11
716/19	518	716/106	1
716/17	267	716/111	3
716/1	693	716/115	17
716/17	267	716/119	4
716/15	126	716/133	1
716/10	470	716/139	2
716/3	275	716/139	1
716/20	73	716/50	1
716/11	334	716/51	1
716/2	571	716/55	10
716/4	1120	716/56	21
716/12	421	716/122	15
716/8	324	716/127	1
716/2	571	716/133	21
716/1	693	716/53	1
716/8	324	716/112	8
716/12	421	716/119	9
716/6	827	716/122	1
716/10	470	716/131	1
716/3	275	716/132	4

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/5	867	716/51	2
716/21	397	716/56	1
716/4	1120	716/102	32
716/5	867	716/102	16
716/1	693	716/103	45
716/13	214	716/106	1
716/1	693	716/112	15
716/15	126	716/113	1
716/7	188	716/121	4
716/4	1120	716/122	9
716/14	114	716/129	17
716/12	421	716/30	1
716/16	387	716/55	1
716/9	187	716/103	4
716/10	470	716/104	8
716/20	73	716/106	1
716/7	188	716/122	13
716/14	114	716/127	3
716/16	387	716/128	20
716/11	334	716/131	2
716/1	693	716/134	1
716/17	267	716/30	2
716/21	397	716/55	42
716/10	470	716/55	5
716/3	275	716/107	8
716/4	1120	716/108	24
716/15	126	716/112	8
716/6	827	716/112	7
716/1	693	716/118	4
716/4	1120	716/119	3
716/16	387	716/129	2
716/17	267	716/138	3
716/2	571	716/50	3
716/7	188	716/50	1
716/19	518	716/53	104
716/11	334	716/53	1
716/12	421	716/103	17
716/16	387	716/106	4
716/1	693	716/107	3
716/20	73	716/136	1
716/17	267	716/121	4
716/12	421	716/125	1
716/19	518	716/55	3

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/4	1120	716/111	1
716/2	571	716/133	1
716/1	693	716/52	1
716/4	1120	716/136	43
716/1	693	716/50	2
716/4	1120	716/51	1
716/21	397	716/56	6
716/1	693	716/103	1
		716/111	1
716/2	571	716/115	1
716/19	518	716/124	1
716/16	387	716/133	1
716/1	693	716/138	5
716/21	397	716/52	7
716/13	214	716/127	1
716/1	693	716/102	2
716/20	73	716/107	1
716/8	324	716/120	1
716/19	518	716/53	20
716/14	114	716/101	1
716/8	324	716/119	4
716/16	387	365/158	1
716/9	187	257/700	1
716/15	126	361/679.31	1
716/10	470	361/56	1
716/17	267	714/25	1
		257/203	3
716/19	518	700/108	1
716/4	1120	714/739	1
716/8	324	711/3	1
716/17	267	257/210	1
716/4	1120	324/762.02	1
716/1	693	714/30	1
716/5	867	324/522	1
716/21	397	700/110	1
716/4	1120	714/732	2
		700/109	1
716/6	827	327/147	1
716/15	126	326/38	1
716/1	693	324/763.01	1
716/21	397	257/773	1
716/20	73	250/307	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/1	693	326/87	1
		257/531	1
716/10	470	712/32	1
716/4	1120	703/16	2
716/11	334	257/773	1
716/14	114	257/758	1
716/1	693	333/12	1
716/4	1120	714/25	1
716/8	324	327/129	1
716/4	1120	324/762.06	2
716/6	827	327/292	1
716/17	267	257/204	1
716/10	470	438/30	1
716/4	1120	430/5	1
716/2	571	700/29	1
716/21	397	250/492.2	4
716/4	1120	348/87	1
716/19	518	324/755.01	2
716/4	1120	714/729	1
716/5	867	702/64	1
716/12	421	327/554	1
716/19	518	600/322	1
716/1	693	326/101	1
716/8	324	439/75	1
716/2	571	438/129	1
716/16	387	326/101	1
716/4	1120	702/59	1
716/1	693	710/313	1
716/9	187	430/5	1
716/15	126	257/737	1
716/8	324	716/103	9
716/13	214	716/112	15
716/8	324	716/114	12
716/2	571	716/135	13
716/4	1120	716/100	1
716/15	126	257/690	1
716/12	421	257/532	1
716/10	470	716/112	25
716/1	693	716/114	6
716/7	188	716/129	7
716/3	275	716/52	4
716/9	187	716/54	3
716/14	114	716/54	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/6	827	716/102	27
716/4	1120	716/103	63
716/6	827	716/107	1
716/4	1120	716/109	17
716/5	867	716/111	21
716/6	827	716/115	14
716/13	214	716/119	1
716/18	478	716/50	1
716/5	867	716/55	11
716/1	693	716/109	5
716/14	114	716/111	1
716/1	693	716/128	1
716/5	867	716/136	20
716/17	267	716/100	2
716/1	693	716/106	25
716/8	324	716/124	13
716/14	114	716/124	1
716/8	324	716/126	2
716/5	867	716/54	3
716/4	1120	716/54	3
716/12	421	716/54	1
716/20	73	716/102	2
716/3	275	716/104	22
		716/115	1
716/14	114	716/118	1
716/11	334	716/126	3
716/10	470	716/132	4
716/1	693	716/135	2
		716/139	5
716/7	188	716/55	4
716/1	693	716/55	8
716/3	275	716/100	1
716/2	571	716/114	17
716/21	397	716/115	1
716/8	324	716/116	3
716/4	1120	716/129	2
		716/133	1
716/2	571	716/134	10
716/10	470	716/54	2
716/17	267	716/102	16
716/13	214	716/115	8
716/16	387	716/116	20
716/6	827	716/117	2

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/7	188	716/124	22
716/5	867	716/127	1
716/15	126	716/130	7
716/21	397	716/51	18
716/8	324	716/52	9
716/17	267	716/55	2
716/19	518	716/103	1
716/16	387	716/105	1
716/12	421	716/108	2
716/11	334	716/110	1
716/17	267	716/110	1
716/18	478	716/114	1
716/12	421	716/116	1
716/16	387	716/123	2
716/10	470	716/129	1
716/1	693	716/116	1
716/13	214	716/55	2
716/2	571	716/55	1
716/19	518	716/100	1
716/6	827	716/111	1
716/1	693	716/113	1
716/17	267	716/117	2
716/18	478	716/102	10
716/1	693	716/51	1
716/14	114	716/129	1
716/1	693	716/55	2
716/19	518	716/132	2
716/17	267	716/137	1
716/1	693	716/30	1
716/18	478	716/106	7
716/4	1120	716/106	2
716/11	334	716/139	2
716/20	73	716/139	1
716/10	470	711/104	1
716/16	387	326/11	1
716/19	518	257/48	1
716/2	571	257/774	1
716/1	693	333/124	1
716/11	334	326/38	1
716/1	693	714/792	1
716/19	518	29/846	1
		326/107	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/8	324	326/38	3
		712/23	1
716/4	1120	382/150	1
716/8	324	326/82	1
		326/8	1
716/4	1120	702/84	1
716/1	693	326/93	2
716/10	470	257/207	1
716/1	693	711/133	1
716/4	1120	714/736	1
716/19	518	438/15	2
716/15	126	174/260	1
716/1	693	174/250	2
716/10	470	327/141	1
716/4	1120	326/38	4
716/1	693	374/121	1
		365/63	1
716/10	470	712/201	1
716/13	214	327/291	1
716/1	693	257/355	1
716/12	421	326/41	8
716/1	693	257/773	3
		700/108	1
716/16	387	326/40	2
716/1	693	327/276	1
		326/81	1
716/4	1120	324/763.01	2
716/8	324	257/773	3
716/20	73	438/510	1
716/2	571	703/5	1
716/13	214	326/96	1
716/16	387	326/16	1
716/10	470	326/97	1
716/1	693	257/730	1
716/4	1120	257/734	1
716/14	114	257/774	1
716/1	693	365/185.23	1
716/17	267	712/43	1
716/2	571	700/121	1
716/20	73	703/2	19
716/8	324	326/101	2
716/6	827	703/2	1
716/16	387	257/208	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/12	421	257/695	1
716/14	114	700/96	1
716/6	827	333/142	1
716/21	397	257/390	1
716/12	421	324/762.06	1
716/10	470	700/121	1
716/4	1120	324/658	1
716/19	518	257/203	1
716/4	1120	326/80	1
716/3	275	326/113	1
716/11	334	438/382	1
716/1	693	257/685	1
716/6	827	326/40	1
716/17	267	327/536	1
716/8	324	365/63	1
716/4	1120	703/15	1
716/10	470	327/334	1
716/4	1120	714/704	1
716/1	693	326/37	1
716/9	187	716/122	27
716/8	324	716/123	27
716/4	1120	716/105	1
716/19	518	716/138	1
716/17	267	716/111	1
716/21	397	250/492.22	2
716/11	334	716/55	10
716/6	827	716/109	4
716/10	470	716/120	17
716/2	571	716/120	4
716/12	421	716/121	3
716/2	571	716/124	4
716/19	518	716/127	1
716/7	188	716/134	1
716/4	1120	716/100	8
716/15	126	716/104	1
716/7	188	716/107	6
716/11	334	716/117	4
716/15	126	716/120	2
716/21	397	716/50	20
716/4	1120	716/52	35
716/5	867	716/106	228
716/19	518	716/112	3
716/2	571	716/119	14

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/12	421	716/130	30
716/19	518	716/139	1
716/7	188	716/51	1
716/11	334	716/108	1
716/16	387	716/113	10
716/8	324	716/115	4
716/13	214	716/118	2
716/19	518	716/119	1
716/7	188	716/127	1
716/18	478	716/129	1
716/2	571	716/129	4
716/4	1120	716/135	2
716/16	387	716/138	1
716/5	867	716/50	2
		716/100	10
716/10	470	716/106	1
716/7	188	716/108	2
716/4	1120	716/110	1
716/2	571	716/112	14
716/9	187	716/112	3
716/5	867	716/113	38
716/10	470	716/117	3
716/14	114	716/117	1
716/18	478	716/120	1
716/9	187	716/123	52
716/4	1120	716/134	1
716/12	421	716/102	7
716/15	126	716/105	1
716/3	275	716/108	3
716/14	114	716/119	2
716/1	693	716/119	22
716/15	126	716/123	1
		716/139	1
716/1	693	716/30	2
716/10	470	716/101	1
716/1	693	716/102	92
716/3	275	716/102	17
716/10	470	716/105	1
716/18	478	716/106	8
716/10	470	716/115	14
716/3	275	716/118	1
716/8	324	716/120	16
716/12	421	716/120	7

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/17	267	716/132	1
716/18	478	716/133	2
716/10	470	716/102	11
716/14	114	716/109	1
716/10	470	716/116	2
		716/121	6
716/3	275	716/122	6
716/17	267	716/127	1
716/19	518	716/51	21
716/21	397	716/54	20
716/18	478	716/105	3
716/5	867	716/111	5
716/15	126	716/100	1
716/7	188	716/125	1
716/11	334	716/126	1
716/17	267	716/50	1
		716/109	1
716/16	387	716/128	3
716/2	571	716/135	2
716/11	334	716/107	1
716/5	867	716/112	4
716/16	387	716/116	3
716/12	421	716/126	26
716/1	693	716/101	10
716/13	214	716/107	1
716/12	421	716/135	3
716/1	693	703/2	4
716/4	1120	438/10	1
716/14	114	438/129	1
716/4	1120	324/66	2
716/17	267	438/129	2
716/5	867	703/13	1
716/4	1120	714/725	3
		382/278	1
716/5	867	438/16	1
		356/237.5	1
716/17	267	326/101	1
716/2	571	326/103	3
		326/40	1
716/1	693	257/666	1
716/21	397	430/5	12
716/4	1120	324/501	2
716/19	518	257/288	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/17	267	326/40	2
716/12	421	438/164	1
716/2	571	257/207	1
716/1	693	257/207	3
716/5	867	257/522	1
716/1	693	710/10	1
716/8	324	257/206	2
716/17	267	326/45	1
716/12	421	257/208	1
716/4	1120	257/391	1
716/8	324	326/113	1
716/4	1120	331/2	1
716/12	421	257/659	2
716/5	867	438/10	1
716/16	387	257/203	2
716/5	867	708/704	1
716/4	1120	324/520	1
716/21	397	355/67	1
716/1	693	341/80	1
716/15	126	333/128	1
716/17	267	326/8	1
716/4	1120	324/678	1
716/12	421	257/529	1
716/1	693	326/39	1
716/20	73	714/726	1
716/13	214	257/774	3
716/1	693	327/152	1
716/14	114	703/14	1
716/1	693	703/23	1
716/2	571	257/203	1
716/12	421	257/508	1
716/4	1120	324/76.19	1
716/16	387	365/185.19	1
716/12	421	716/117	7
716/17	267	716/124	1
716/11	334	716/129	2
716/10	470	438/128	1
716/14	114	327/156	1
		257/207	1
716/15	126	703/2	1
716/1	693	361/679.32	1
716/20	73	716/52	5
716/2	571	716/105	9

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/4	1120	716/105	2
716/17	267	716/106	2
716/7	188	716/111	3
716/14	114	716/113	5
716/4	1120	716/126	1
716/15	126	716/102	7
716/3	275	716/105	4
716/2	571	716/111	13
716/13	214	716/114	9
716/5	867	716/115	124
716/15	126	716/117	1
716/1	693	716/117	10
716/9	187	716/121	6
716/13	214	716/122	7
716/11	334	716/124	9
716/6	827	716/126	1
716/5	867	716/129	1
716/10	470	716/130	5
716/1	693	716/137	10
716/19	518	716/50	11
716/21	397	716/53	63
716/4	1120	716/101	3
716/18	478	716/116	4
716/3	275	716/120	1
716/11	334	716/121	3
716/9	187	716/124	7
716/11	334	716/135	1
716/4	1120	716/104	17
716/13	214	716/109	1
716/7	188	716/117	4
716/9	187	716/118	1
716/5	867	716/119	3
716/4	1120	716/130	3
716/11	334	716/132	1
716/4	1120	716/136	252
		716/139	2
716/16	387	716/50	1
716/2	571	716/106	18
		716/108	23
716/1	693	716/108	10
716/8	324	716/118	8
716/3	275	716/119	2
716/8	324	716/121	9

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DISPOSITION CLASSIFICATION(S) OF PATENTS
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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/14	114	716/123	2
716/17	267	716/130	1
716/13	214	716/139	1
716/9	187	716/55	5
716/12	421	716/55	3
716/13	214	716/103	3
716/6	827	716/114	74
716/10	470	716/114	40
716/3	275	716/126	1
716/13	214	716/127	8
716/4	1120	716/106	153
716/9	187	716/108	2
716/18	478	716/108	2
716/17	267	716/122	3
716/5	867	716/124	2
716/12	421	716/126	52
716/13	214	716/129	63
716/2	571	716/132	57
716/12	421	716/50	1
		716/51	1
716/1	693	716/101	16
716/16	387	716/104	13
716/7	188	716/110	1
716/11	334	716/113	12
716/4	1120	716/114	4
716/10	470	716/126	3
716/5	867	716/126	5
716/15	126	716/131	1
716/1	693	716/132	8
716/2	571	716/136	2
716/20	73	716/53	1
716/1	693	716/110	4
716/15	126	716/137	23
716/21	397	716/50	24
716/16	387	716/108	1
716/11	334	716/119	4
716/1	693	716/127	1
716/12	421	716/129	4
716/5	867	716/113	1
716/8	324	716/118	7
716/4	1120	716/132	3
716/12	421	716/102	1
716/8	324	716/103	1

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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/18	478	716/104	26
716/17	267	716/103	1
716/19	518	716/109	1
716/12	421	716/110	1
716/10	470	716/122	4
716/2	571	716/132	4
716/21	397	716/51	25
716/19	518	716/52	15
		716/56	2
716/16	387	716/101	5
716/8	324	716/111	1
716/15	126	716/135	1
716/6	827	326/96	1
716/4	1120	324/762.01	3
		324/519	1
		700/121	3
716/5	867	324/762.09	1
716/6	827	327/277	1
		327/285	1
716/1	693	700/121	2
716/21	397	382/144	1
716/19	518	700/121	6
716/4	1120	324/750.3	1
716/21	397	438/14	1
716/13	214	257/775	1
716/21	397	438/94	1
		703/12	1
716/8	324	257/207	4
716/21	397	430/22	4
716/11	334	700/121	1
716/5	867	702/189	1
716/1	693	365/51	1
		327/149	1
716/3	275	326/41	1
716/6	827	714/726	1
716/7	188	438/129	1
716/8	324	257/208	1
716/5	867	700/104	1
		333/185	1
716/1	693	257/506	1
		327/33	1
716/19	518	382/144	3
716/4	1120	702/94	1

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DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/19	518	700/95	1
716/7	188	709/208	1
716/2	571	438/17	1
716/17	267	326/21	1
716/6	827	326/94	1
716/5	867	333/246	1
716/4	1120	712/216	1
		438/12	1
		706/20	1
716/16	387	326/41	19
716/1	693	326/83	1
716/15	126	361/720	1
716/1	693	438/17	1
716/13	214	257/773	1
716/4	1120	438/15	2
716/12	421	257/776	1
716/4	1120	438/17	1
716/1	693	702/183	1
		711/104	1
716/4	1120	324/750.15	2
		327/267	1
716/13	214	257/207	2
716/3	275	709/223	1
716/10	470	257/439	1
716/1	693	708/627	1
716/21	397	382/141	1
716/8	324	438/622	1
716/3	275	716/106	6
716/10	470	716/127	2
716/7	188	438/692	1
716/15	126	333/4	1
716/17	267	257/369	1
716/5	867	716/30	1
716/17	267	716/52	1
716/7	188	716/101	2
716/6	827	716/104	29
716/13	214	716/104	3
716/6	827	716/106	15
716/11	334	716/106	6
716/20	73	716/111	1
716/4	1120	716/112	61
716/17	267	716/121	6
716/15	126	716/127	1

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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/18	478	716/130	1
716/8	324	716/53	5
716/20	73	716/53	2
716/3	275	716/55	4
716/17	267	716/108	6
716/9	187	716/111	2
716/11	334	716/120	8
716/14	114	716/122	4
716/20	73	716/55	6
716/5	867	716/103	50
716/17	267	716/104	14
716/4	1120	716/111	27
716/12	421	716/112	12
716/4	1120	716/117	6
716/7	188	716/123	10
716/13	214	716/130	3
716/1	693	716/133	7
716/19	518	716/54	18
716/2	571	716/103	47
716/12	421	716/107	1
716/16	387	716/108	4
716/4	1120	716/115	64
716/15	126	716/115	10
716/3	275	716/116	1
716/9	187	716/119	22
716/1	693	716/125	2
716/12	421	716/129	65
716/3	275	716/101	1
716/12	421	716/106	1
		716/111	5
716/2	571	716/113	34
716/13	214	716/126	5
716/2	571	716/127	1
716/11	334	716/128	1
716/6	827	716/134	9
		716/136	5
716/10	470	716/50	2
716/2	571	716/56	1
716/6	827	716/103	39
716/18	478	716/104	149
716/5	867	716/107	41
		716/109	11
716/14	114	716/112	2

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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/15	126	716/122	5
716/8	324	716/125	2
716/12	421	716/128	8
716/19	518	716/132	1
716/8	324	716/135	1
716/1	693	716/104	43
716/9	187	716/113	10
716/2	571	716/121	2
716/12	421	716/124	3
716/13	214	716/124	6
716/14	114	716/130	30
716/19	518	716/52	87
716/5	867	716/56	1
716/7	188	716/103	11
716/5	867	716/108	24
		716/110	1
716/19	518	716/115	2
		716/118	1
716/10	470	716/118	4
716/6	827	716/119	2
716/14	114	716/121	1
716/12	421	716/123	6
716/17	267	716/54	1
716/1	693	716/129	1
716/13	214	716/100	1
716/17	267	716/108	1
		716/114	1
716/16	387	716/117	2
716/17	267	716/104	2
716/1	693	716/109	1
716/16	387	716/134	1
716/2	571	716/103	1
716/1	693	716/106	3
716/16	387	716/138	53
716/20	73	716/104	1
716/13	214	716/126	3
716/3	275	716/50	1
716/4	1120	716/50	1
716/12	421	716/104	2
716/6	827	716/114	1
716/18	478	716/132	3
		716/103	4
716/3	275	716/103	3

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Generated by Data Control Division

Source Classification	Number of ORs	New Classification	Number of ORs
716/1	693	716/104	1
716/14	114	716/130	6
716/13	214	716/134	1
716/6	827	716/113	12
716/1	693	333/24 R	1
716/10	470	438/15	1
716/19	518	29/847	1
716/16	387	257/206	1
716/1	693	257/690	1
716/4	1120	705/59	2
716/3	275	710/8	1
716/5	867	174/257	1
716/1	693	703/14	2
716/2	571	700/99	1
716/6	827	326/38	2
716/8	324	323/234	1
716/21	397	438/703	1
716/8	324	710/8	1
716/19	518	438/129	1
716/5	867	700/108	1
716/4	1120	327/512	1
716/10	470	257/774	1
716/18	478	709/223	1
716/2	571	326/41	1
716/21	397	347/262	1
716/4	1120	709/226	1
716/19	518	326/38	1
716/10	470	700/110	1
716/4	1120	714/738	4
716/11	334	382/149	1
716/12	421	257/665	1
716/1	693	713/160	1
716/12	421	257/773	1
716/19	518	174/257	1
716/21	397	365/230.04	1
716/3	275	326/40	1
716/8	324	326/49	1
716/14	114	713/300	1
716/10	470	257/203	1
716/1	693	365/227	1
716/21	397	702/82	1
716/4	1120	714/727	2
716/12	421	326/101	1

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Source Classification	Number of ORs	New Classification	Number of ORs
716/4	1120	702/35	1
716/17	267	333/4	1
716/21	397	250/310	2
716/7	188	382/149	1
716/8	324	360/46	1
716/17	267	257/208	1
		714/7	1
716/16	387	326/38	30
716/1	693	438/599	1
716/10	470	257/206	2
716/3	275	705/51	1
716/1	693	326/30	1
716/21	397	250/396 R	3
716/17	267	326/28	1
		257/360	1
716/16	387	257/776	1
716/13	214	709/223	1
716/5	867	326/46	1
716/4	1120	703/21	1
716/2	571	716/117	3
716/11	334	716/134	1
716/16	387	716/121	9
716/18	478	714/30	1
716/1	693	438/128	1
		323/271	1

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C. CHANGES TO THE USPC-TO-IPC CONCORDANCE

USPC		IPC	
Class	Subclass	Subclass	Notation
716	30	G06F	17/50
	50-56	G06F	17/50
	100-102	G06F	17/50
	103	G06F	9/45
	104-105	G06F	17/50
	106-109	G06F	9/455
			17/50
	110	G06F	17/50
	111-113	G06F	9/455
			17/50
	114-131	G06F	17/50
	132-135	G06F	9/455
			17/50
	136	G06F	11/22
			17/50
	137-138	G06F	17/50
	139	G06F	15/04
			17/50

D. CHANGES TO THE DEFINITIONS

CLASS 257 – ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID-STATE DIODES)

Definitions Modified:

Class Definition: Under **SECTION IV – REFERENCES TO OTHER CLASSES**, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 50 through 56 for design and analysis of a semiconductor mask or reticle and subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

D. CHANGES TO THE DEFINITIONS

CLASS 326 – ELECTRONIC DIGITAL LOGIC CIRCUITRY

Definitions Modified:

Subclass 41: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

Subclass 47: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

Subclass 101: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

D. CHANGES TO THE DEFINITIONS

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

D. CHANGES TO THE DEFINITIONS

CLASS 327 – MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS

Definitions Modified:

Subclass 565: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

D. CHANGES TO THE DEFINITIONS

CLASS 340 – COMMUNICATIONS: ELECTRICAL

Definitions Modified:

Subclass 14.3: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclass 116 for mapping circuit design to programmable logic devices (PLDs).

D. CHANGES TO THE DEFINITIONS

CLASS 359 – OPTICAL: SYSTEMS AND ELEMENTS

Definitions Modified:

Subclass 107: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 361 – ELECTRICITY: ELECTRICAL SYSTEMS AND DEVICES

Definitions Modified:

Subclass 600: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 505 – SUPERCONDUCTOR TECHNOLOGY: APPARATUS, MATERIAL, PROCESS

Definitions Modified:

Subclass 170: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, for pertinent subclass(es) as determined by schedule review.

D. CHANGES TO THE DEFINITIONS

CLASS 700 – DATA PROCESSING: GENERIC CONTROL SYSTEMS OR SPECIFIC APPLICATIONS

Definitions Modified:

Subclass 97: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

Subclass 121: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 30 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

D. CHANGES TO THE DEFINITIONS

CLASS 703 – DATA PROCESSING: STRUCTURAL DESIGN, MODELING, SIMULATION, AND EMULATION

Definitions Modified:

Class Definition: Under **SECTION II – REFERENCES TO OTHER CLASSES**, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 101-109 for logic design processing for integrated circuit.

Subclass 19: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 108 and 113 for analyzing the timing delay of a circuit design.

D. CHANGES TO THE DEFINITIONS

CLASS 704 – DATA PROCESSING: SPEECH SIGNAL PROCESSING, LINGUISTICS, LANGUAGE TRANSLATION, AND AUDIO COMPRESSION/DECOMPRESSION

Definitions Modified:

Subclass 2: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 103 through 105 for translation of computer program in designing and analyzing circuits and semiconductor mask.

D. CHANGES TO THE DEFINITIONS

CLASS 707 – DATA PROCESSING: DATABASE, DATA MINING, AND FILE MANAGEMENT OR DATA STRUCTURES

Definitions Modified:

Subclass 790: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 50 through 56 for design of semiconductor masks and subclasses 100 through 139 for circuit design.

D. CHANGES TO THE DEFINITIONS

CLASS 708 – ELECTRICAL COMPUTERS: ARITHMETIC PROCESSING AND CALCULATING

Definitions Modified:

Class Definition: Under SECTION II – REFERENCES TO OTHER CLASSES, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 709 – ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MULTICOMPUTER DATA TRANSFERRING

Definitions Modified:

Class Definition: Under SECTION II – REFERENCES TO OTHER CLASSES, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 712 – ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING (E.G., PROCESSORS)

Definitions Modified:

Class Definition: Under SECTION III – REFERENCES TO OTHER CLASSES, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 204: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 209: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

Subclass 227: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 232: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 241: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 242: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

D. CHANGES TO THE DEFINITIONS

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 248: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 713 – ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT

Definitions Modified:

Class Definition: Under SECTION II – REFERENCES TO OTHER CLASSES, SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 714 – ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY

Definitions Modified:

Subclass 28: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 33: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

Subclass 37: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

D. CHANGES TO THE DEFINITIONS

CLASS 716 – COMPUTER-AIDED DESIGN AND ANALYSIS OF CIRCUITS AND SEMICONDUCTOR MASKS

Definitions Abolished

Subclasses:

1-21

Definitions Modified

In this (Class 716) and other classes within the U.S. Patent Classification System where the class title for Class 716 appears:

Delete:

DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK

Insert:

COMPUTER-AIDED DESIGN AND ANALYSIS OF CIRCUITS AND SEMICONDUCTOR MASKS

Class Definition:

Delete:

The entire Class Definition

Insert:

SECTION I - CLASS DEFINITION

GENERAL STATEMENT OF THE CLASS SUBJECT MATTER

This class provides for computer-based tools, i.e., electrical data processing apparatus and corresponding methods for the following subject matter:

D. CHANGES TO THE DEFINITIONS

A. Processes or apparatus for sketching, designing, and analyzing circuits or circuit components.

B. Processes or apparatus for planning, designing, analyzing, and devising a template used for creating a mask on a semiconductor wafer.

SCOPE OF THE CLASS

(1) Note. Processes and apparatus for the use of digital components in various types of digital logic circuitries or active electrical nonlinear circuits or devices are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(2) Note. Processes and apparatus for connections of electrical components on a printed circuit board are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(3) Note. Processes and apparatus for computer-controlled semiconductor fabrication are classified elsewhere. See the SEE OR SEARCH CLASS notes below.

(4) Note. Significantly claimed apparatus external to this class, claimed in combination with apparatus under the class definition, which perform data processing circuit design and analysis, are classified in the class appropriate to the external device unless specifically excluded therefrom.

(5) Note. Nominally claimed apparatus external to this class in combination with apparatus under the class definition is classified in this class unless provided for in the appropriate external class.

SECTION II - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

204, Chemistry: Electrical and Wave Energy, subclasses 298.01 through 298.39 for coating, forming, or etching apparatus using atomic particles.

250, Radiant Energy, subclasses 491.1 through 492.3 for irradiating object or material and the ion or electron beam irradiation, per se.

257, Active Solid-State Devices (e.g., Transistors, Solid-State Diodes), appropriate subclasses for detail structure of active solid-state devices.

324, Electricity: Measuring and Testing, appropriate subclasses for measuring and testing of electrical devices, in general, particularly subclasses 210 through 212 for magnetic information storage element testing and subclasses 762.01 through 762.1 for testing of a semiconductor device.

D. CHANGES TO THE DEFINITIONS

326, Electronic Digital Logic Circuitry, appropriate subclasses for the use of digital components in various types of electronic digital logic circuitries; particularly subclass 10 for the redundancy of circuit components or devices; subclasses 37 through 39, 41, and 47 for the use of programmable devices and their layout interconnections; subclass 38 for the details of setting or programming of interconnections in multifunctional or programmable digital logic circuitry; and subclasses 41 and 47 for significant layout or layout interconnections.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for the use of electrical components in various types of active electrical nonlinear circuits or devices.

340, Communications: Electrical, subclass 14.3 for the use of programmable devices in selective communication.

345, Computer Graphics Processing and Selective Visual Display Systems, appropriate subclasses for creation and manipulation of graphical objects.

361, Electricity: Electrical Systems and Devices, subclasses 760 through 783 for the connections of electrical components on a printed circuit board.

430, Radiation Imagery Chemistry: Process, Composition, or Product Thereof, subclass 5 for radiation masks used in radiation imaging of semiconductor devices.

438, Semiconductor Device Manufacturing: Process, appropriate subclasses for the process of manufacturing semiconductor devices.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 121 for computer-controlled semiconductor fabrication.

702, Data Processing: Measuring, Calibrating, or Testing, appropriate subclasses for data processing testing, in general.

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 14 through 16 for circuit and logic simulation.

706, Data Processing: Artificial Intelligence, appropriate subclasses for data processing utilizing knowledge base, rule base, and neural networks.

708, Electrical Computers: Arithmetic Processing and Calculating, appropriate subclasses for arithmetic processing and calculating computer.

714, Error Detection/Correction and Fault Detection/Recovery, appropriate subclasses for reliability and availability, particularly subclasses 25 through 46

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for fault locating; subclass 30 for scan path testing; and subclasses 724 through 745 for testing and detecting error/fault in one or more circuit components.

Definitions Established

SUBCLASSES

30 NANOTECHNOLOGY RELATED INTEGRATED CIRCUIT DESIGN:
This subclass is indented under the class definition. Subject matter comprising means or steps for computer aided design related to the representation, modeling, or design of integrated circuits involving nanotechnology.

50 DESIGN OF SEMICONDUCTOR MASK OR RETICLE:
This subclass is indented under the class definition. Subject matter comprising means or steps for using computer-based tools to aid in planning or devising a template of a circuit pattern to be used for transferring onto a semiconductor wafer.

51 Analysis and verification (process flow, inspection):
This subclass is indented under subclass 50. Subject matter comprising means or steps for analyzing or verifying that a mask or pattern layout conforms to manufacturing-specific design rules or processes.

52 Defect (including design rule checking):
This subclass is indented under subclass 51. Subject matter comprising means or steps for analyzing or verifying mask or pattern layout by performing layout versus schematic analysis or design rule checking.

53 Optical proximity correction (including RET):
This subclass is indented under subclass 51. Subject matter comprises means or steps for compensating for image errors due to diffraction or photoprocess effects.

(1) Note. Examples of optical proximity correction of this subclass type include adding serifs, hammerheads, etc., to the mask pattern or layout pattern so as to overcome optical proximity effects when fabricating the circuit at a higher resolution than normally handled by the lithographic tools.

54 Manufacturing optimizations:
This subclass is indented under subclass 50. Subject matter comprising means or steps for improving physical circuit design representations specifically for fabrication or manufacture (i.e., design for manufacture (DFM)) including lithography-based design improvements.

55 Layout generation (polygon, pattern feature):
This subclass is indented under subclass 50. Subject matter comprising means or steps for generating a mask or pattern layout of the circuit design for fabrication or manufacturing process.

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56 Yield:
This subclass is indented under subclass 50. Subject matter comprising means or steps for predicting yield for the circuit design, such as using aerial image simulation or process specific simulation.

100 INTEGRATED CIRCUIT DESIGN PROCESSING:
This subclass is indented under the class definition. Subject matter comprising means or steps for using computer-based tools to aid in logical and physical design and layout analysis.

101 Logic design processing:
This subclass is indented under the subclass 100. Subject matter comprising means or steps wherein a system, functional, or architectural level design representation is analyzed or evaluated, generally in terms of inputs, outputs, and stimuli, in a manner which allows for the design representation to be operated on at various levels by design tools.

(1) Note. Subject matter of this subclass type generates design representations (such as High Definition Language (HDL) or Register Transfer Logic (RTL) level representations) that may be analyzed in greater detail, perform other logical behavioral analyses, such as netlist processing (functional and interconnection representations), synthesis, simulations, translations, and verifications.

(2) Note. Subject matter of this subclass type usually consists of higher level description representations and may include higher level languages, such as VHDL, C language, graphical representations, and utilization of libraries of behavioral descriptions.

102 Design entry:
This subclass is indented under subclass 101. Subject manner comprising means and steps for generating, analyzing, editing, revising, or modifying a high hardware description language, schematic, or other circuit design representation at various levels of abstraction for use by an electronic design automation (EDA) tool.

103 Translation (logic-to-logic, logic-to-netlist, netlist processing):
This subclass is indented under subclass 101. Subject manner comprising means and steps for converting an original circuit design representation to a target circuit design representation which performs the same function as the original, e.g., netlist creation (a representation of elements and their connections) or a conversion between different programming languages used for circuit representations.

104 Logic circuit synthesis (mapping logic):
This subclass is indented under subclass 101. Subject matter comprising means or steps for determining actual circuit elements and their arrangements which provide desired logical operations.

(1) Note. Subject matter may comprise means and steps for implementing a logic or high level circuit design in which a netlist representation of a circuit design is

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converted into a representation of a target circuit design or a target circuit product or a product family.

(2) Note. Subject matter of this subclass type is sometimes called “technology mapping”.

105 With partitioning:
This subclass is indented under subclass 104. Subject manner including means or steps for dividing a circuit design into subsections.

106 Design verification (functional simulation, model checking):
This subclass is indented under subclass 101. Subject manner comprising means or steps for checking, evaluating, or verifying functionality or logic of a circuit design.

107 Equivalence checking:
This subclass is indented under subclass 106. Subject manner comprising means or steps for comparing design representations to design requirements or preconditions.

108 Timing verification (timing analysis):
This subclass is indented under subclass 106. Subject manner comprising means or steps for performing timing analysis or timing verification on the logic or high level circuit design.

(1) Note. Steps may include verification and analysis of the logical, sequential flow of signals or switching operations of circuit element representations using methods such as finite state machines (FSMs), binary decision diagrams (BDDs), or other methods which may verify or analyze the logical state of signals or circuit elements.

109 Power estimation:
This subclass is indented under subclass 106. Subject manner comprising means or steps for analyzing, evaluating, or estimating power consumption of a circuit design.

110 Physical design processing:
This subclass is indented under the subclass 100. Subject matter comprising means or steps for creating an actual, physical, geometrical design of an integrated circuit.

(1) Note. Steps may include the entry or creation of floorplans of circuit elements, placing and routing between circuit elements, optimization, and verifications techniques which prepare a circuit design prior to mask making and integrated circuit manufacture.

(2) Note. This subclass is intended to include circuit design representations that include the physical nature of integrated circuit elements such as transistors, resistors, capacitors, diodes, wires, or signal traces, interactions of circuit elements with respect to each other, or the physical medium in which they will be formed.

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111 Verification:
This subclass is indented under subclass 110. Subject matter comprising means or steps for checking and confirming the circuit component layout or routing for consistency or correctness.

112 Defect analysis:
This subclass is indented under subclass 111. Subject matter wherein the design verification comprises means or steps for determining layout or routing compliance with specifications, design rule requirements, etc.

(1) Note. Subject matter of this subclass type includes, for example, Layout Versus Schematic (LVS) and Design Rule Checking (DRC) techniques.

113 Timing analysis:
This subclass is indented under subclass 111. Subject matter wherein the design verification is confirmed based on timing constraints such as delay or slack of the circuit components with respect to layout/routing, critical paths, static timing analysis, etc.

114 Buffer or repeater insertion:
This subclass is indented under subclass 113. Subject matter wherein the findings of timing analysis are addressed by the insertion of circuit components such as buffers, repeaters, inverters, scan chains, etc.

115 Noise (e.g., crosstalk, electromigration, etc.):
This subclass is indented under subclass 111. Subject matter wherein the design verification involves detecting or evaluating possible sources of undesired signal components, e.g., parasitic parameters, victim/aggressor nets, width/length characteristics, etc.

116 Mapping circuit design to programmable logic devices (PLDs):
This subclass is indented under subclass 110. Subject matter comprising means or steps for automatically transforming or converting a circuit design into a programmable implementation.

(1) Note. Programmable logic devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

(2) Note. Transformed or converted circuit designs of this subclass type include, for example, specifications, high-level descriptions, netlists, Boolean expressions, etc. Programmable implementations of this subclass type include, for example, configurable logic blocks (CLBs), look-up tables (LUTs), registers, etc.

117 Configuring PLDs (including data file, bitstream generation, etc.):
This subclass is indented under subclass 116. Subject matter wherein a file or bitstream is generated from the mapped PLD which defines how the circuit components on the PLD are arranged, placed, routed, etc.

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118 Floorplanning:
This subclass is indented under subclass 110. Subject matter comprising means or steps for placing circuit block units or cells on a layout area of an LSI or PCB.

(1) Note. Floorplanning of this subclass type occurs at the initial designing stage.

119 Placement or layout:
This subclass is indented under subclass 118. Subject matter comprising means or steps for refining the floorplan, i.e., refining the position assignment or the size or the shape of the circuit block units or cells.

120 Power distribution:
This subclass is indented under subclass 119. The subject matter comprising means or steps for refining the position assignment, size, or shape of circuit block units, cells, or clock tree structures (components) for the purpose of gaining a desired placement of components and the respective power distribution.

121 For PLDs:
This subclass is indented under subclass 119. The subject matter comprising means or steps for refining the position assignment, size, or shape of circuit block units, cells, or (programmable) logic elements on a programmable logic device, such as FGPAs, ASICs, etc.

(1) Note. Programmable Logic Devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

122 Constraint-based:
This subclass is indented under 119. Subject matter wherein the arrangement of circuit block units or circuit components must satisfy one or more positional assignment restraints.

123 Iteration:
This subclass is indented under subclass 119. Subject matter comprising means or steps for repeatedly adjusting and evaluating the position assignment, size, or shape of the circuit block units or cells to improve the efficiency of the floorplan.

124 With partitioning:
This subclass is indented under subclass 119. Subject matter comprising means or steps for dividing the circuit design into a set of smaller sub-circuits.

125 With partitioning:
This subclass is indented under subclass 118. Subject matter comprising means or steps for dividing the circuit design into a set of smaller sub-circuits.

126 Routing:
This subclass is indented under subclass 110. Subject matter comprising means or steps for determining interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins).

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127 Power (voltage islands):
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the interconnection paths with respect to power to or between circuit blocks, cells, or components of an integrated circuit.

128 PLDs:
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the interconnection of paths to or between logic elements of a programmable logic device (PLD), including the wiring within the logic elements, and the wiring, or switching techniques used for the connections between elements.

(1) Note. Programmable Logic Devices (PLDs) include programmable logic arrays (PLAs), field programmable gate arrays (FPGAs), gate arrays, etc.

129 Global:
This subclass is indented under subclass 126. Subject matter comprising means or steps for evaluating or determining the shortest interconnection paths or minimizing the number of channels required for placing the conductor paths between nets.

130 Detailed:
This subclass is indented under subclass 126. Subject matter comprising means or steps for determining the wiring route within a specified circuit region.

(1) Note. A detailed router searches and finds the actual geometric layout of a specific circuit region and considers only one region at a time as opposed to global router which considers the entire circuit regions of the layout.

(2) Note. Detailed routing includes channel routing and switch box routing.

131 With partitioning:
This subclass is indented under subclass 126. Subject matter comprising means or steps wherein determining the interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins) involves dividing or sectioning the layout.

132 Optimization:
This subclass is indented under subclass 100. Subject matter comprising means or steps for improving a circuit design by improving the logic design representation through the use of an algorithm or other compaction or minimization method, or by improving the physical circuit design by specific constraints or criteria.

133 For power:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to power to or between circuit elements.

134 For timing:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to timing to or between circuit elements.

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135 For area:
This subclass is indented under subclass 132. Subject matter wherein the means or steps for improving a circuit design relate to the layout of design elements on a circuit design space.

136 Testing or evaluating:
This subclass is indented under subclass 100. Subject matter comprising means or steps for determining, i.e., testing or evaluating, the performance of the circuit or component design.

137 PCB, MCM design:
This subclass is indented under subclass 100. Subject matter comprising means or steps for sketching, outlining, or defining the layout or routing of circuit components on a printed circuit board (PCB), printed wiring board (PWB), or multi-chip module (MCM).

138 System-on-chip design:
This subclass is indented under subclass 100. Subject matter comprising means or steps for sketching, outlining, or defining the layout or routing of circuit components contained on a single chip.

139 Layout editor (with ECO, reuse, GUI):
This subclass is indented under subclass 100. Subject matter comprising means or steps for interactively using a workstation or graphical user interface (GUI) to sketch, outline, or define the layout or routing of circuit components.

FOREIGN ART COLLECTIONS

FOR 100 CIRCUIT DESIGN:
Foreign art collection including subject matter comprising means or steps for sketching or outlining of layout of circuit components.

FOR 101 Optimization (e.g., redundancy, compaction):
Foreign art collection including subject matter comprising means or steps for improving the layout of the designed circuit components as far as possible.

(1) Note. Examples of the circuit design improvements are global redundancy or compaction of the designed circuit layout such that preserving the integrity of the original circuit design in compliance with design rule requirements.

FOR 102 Translation (e.g., conversion, equivalence):
Foreign art collection including subject matter comprising means or steps for converting an original circuit design data to a target circuit design data having different circuit components while performing the same function as the original circuit design by utilizing a rule group for the conversion.

(1) Note. Rule group, design rule, or design specification have substantially the same meaning. They refer to a set of regulations which define the acceptable dimensions and electrical characteristics achievable in a fabrication process.

D. CHANGES TO THE DEFINITIONS

FOR 103 Testing or evaluating:

Foreign art collection including subject matter comprising means or steps for determining (i.e., evaluating) the performance of the designed circuit components.

FOR 104 Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width):

Foreign art collection including subject matter comprising means or steps for checking and confirming the circuit component s layout for consistency of the functional and logical correctness.

FOR 105 Timing analysis (e.g., delay time, path delay, latch timing):

Foreign art collection including subject matter wherein the design verification is confirmed based on timing constraints such as delay or latch timing of the circuit components.

FOR 106 Partitioning (e.g., function block, ordering constraint):

Foreign art collection including subject matter comprising means or steps for dividing the circuit design into a set of smaller subcircuits arranged in a logical hierarchical structure.

FOR 107 Floorplanning:

Foreign art collection including subject matter comprising means or steps for enabling exact judgment of accommodation feasibility of using circuit block units or cells on a layout area of an LSI or PCB at the initial designing stage.

FOR 108 Detailed placement (i.e., iterative improvement):

Foreign art collection including subject matter comprising means or steps for refining the position assignment, the size or the shape of the circuit block units or cells, and evaluating repeatedly the position assignment of the block units or cells until all the cells are replaced as efficiently as possible in a refined portion of the floor planned layout of a PCB or an LSI.

FOR 109 Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance):

Foreign art collection including subject matter wherein the arrangement of circuit block units or circuit components must satisfy one or more positional assignment restraints.

FOR 110 Layout editor (e.g., updating):

Foreign art collection including subject matter comprising means or steps for revising or modifying the circuit layout interactively by utilizing graphical representations such as icons or menus.

FOR 111 Routing (e.g., routing map, netlisting):

Foreign art collection including subject matter comprising means or steps for determining the interconnections or path nets between circuit blocks or circuit components and input/output bonding pads (pins).

(1) Note. Connection of terminals or nets at the periphery of a block to the terminals of another block is called a netlist.

(2) Note. Netlisting or process of generating a netlist is included in this subclass.

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FOR 112 Global routing (e.g., shortest path, dead space, or duplicate trace elimination):
Foreign art collection including subject matter comprising means or steps for evaluating or determining the shortest interconnection paths or minimizing the number of channels required for placing the conductor paths between nets.

(1) Note. In global routing, the wiring path capacities in a path net or between plural path routing regions and their relationships are usually modeled as graph or trees.

(2) Note. Procedures for determining the shortest paths may include, for example, Maze routing algorithm, Lee's algorithm, Soukup's algorithm, Hadlock's algorithm, or Steiner tree-based algorithm.

FOR 113 Detailed routing (e.g., channel routing, switch box routing):
Foreign art collection including subject matter comprising means or steps for determining the wiring route within a specified circuit region.

(1) Note. A detailed router searches and finds the actual geometric layout of a specific circuit region and considers only one region at a time as opposed to global router which considers the entire circuit regions of the layout.

(2) Note. Detailed routing includes channel routing and switch box routing.

FOR 114 PCB wiring:
Foreign art collection including subject matter including the routing paths or wiring of circuit components on a printed circuit board.

FOR 115 PLA, PLD, FPGA or MCM:
Foreign art collection including subject matter wherein the circuit components are programmable logic arrays or devices, field programmable gate arrays, or multichip modules.

FOR 116 Programmable integrated circuit (e.g., basic cell, standard cell, macrocell):
Foreign art collection including subject matter wherein the designed circuit utilizes a high-level circuit element such as an arithmetic or logical component selectively operable (i.e., programmable component) to perform a given or required specific combinational function.

FOR 117 Logical circuit synthesizer:
Foreign art collection including subject matter comprising means or steps for automatically transforming a high-level design (e.g., functional specification or functional-level logic such as Boolean expression, truth table, or standard macro logic) into its hardware implementation.

FOR 118 DESIGN OF SEMICONDUCTOR MASK:
Foreign art collection including subject matter comprising means or steps for planning or devising a template used for etching circuit pattern on semiconductor wafers.

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FOR 119 Mesh generation:

Foreign art collection including subject matter comprising means or steps for determining or approximating the surface contour of the mask by mathematical model or algorithm such as numerical analysis.

(1) Note. The shape or boundary of the mask is divided or segmented into rectangular, triangular, or polygon grids for approximation, for example, by differential equations algorithm.

FOR 120 Pattern exposure:

Foreign art collection including subject matter including means or steps for tracing or drawing an electronic pattern on a semiconductor wafer or mask with particle beam.

(1) Note. Examples of particle beams are ion beams, electron beams, or e-beams.

D. CHANGES TO THE DEFINITIONS

CLASS 717 – DATA PROCESSING: SOFTWARE DEVELOPMENT, INSTALLATION, AND MANAGEMENT

Definitions Modified:

Subclass 104: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 50 through 56 for design and analysis of a semiconductor mask or reticle and subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.

Subclass 106: Under SEE OR SEARCH CLASS:

Delete:

The reference to Class 716

Insert:

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, subclasses 50 through 56 for design and analysis of a semiconductor mask or reticle and subclasses 100 through 139 for the design and analysis of circuit systems and integrated circuit structure by data processing and computer programming techniques.