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Paper No. 107
Date: October 14, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

OPENSKY INDUSTRIES, LLC,
INTEL CORPORATION,
Petitioners,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2021-01064
Patent 7,725,759 B2

Before THOMAS L. GIANNETTI, BRIAN J. MCNAMARA, and JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

ORDER
Decision on Remand
Assessing Merits at Institution

I. INTRODUCTION

OpenSky Industries, LLC ("Petitioner") filed a Petition (Paper 2, "Pet.") requesting institution of *inter partes* review of claims 1, 14, 17, 18, 21, 22, and 24 ("the challenged claims") of U.S. Patent No. 7,725,759 B2 (Ex. 1001, "the '759 patent"). VLSI Technology LLC ("Patent Owner") opposed. Paper 9 (Preliminary Response, "Prelim. Resp."); Paper 16 (Preliminary Sur-Reply); *see also* Paper 13 (Petitioner's Preliminary Reply). On December 23, 2021, we instituted review. Paper 17 ("Institution Decision", or "Inst."). In addition, Intel Corporation filed a petition requesting *inter partes* review of claims 1, 14, 17, 18, 21, 22, and 24 of the '759 patent. IPR2022-00366, Paper 3. On June 8, 2022, we instituted review in IPR2022-00366 and joined Intel Corporation as a petitioner in this proceeding. Paper 43.

The Director initiated review of our Institution Decision on June 7, 2022. Paper 41. On October 4, 2022, the Director remanded the decision to us, directing us to issue an order by October 18, 2022, "on whether the record before the Board prior to institution indicates that the Petition presents a compelling, meritorious challenge" as consistent with the June 21, 2022, Director's Memorandum ("Memorandum").[1] Paper 102 ("Director Remand"), 49. The Director ordered us to apply the Memorandum's guidance, specifically that "[c]ompelling, meritorious challenges are those in which the evidence, if unrebutted at trial, would plainly lead to a conclusion

[1] *Available at* https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

that one or more claims are unpatentable by a preponderance of the evidence." *Id.* (quoting Memorandum at 4) (alteration in original).

Having evaluated the record prior to institution, we conclude that the Petition presents a compelling, meritorious challenge.

A. THE '759 PATENT

The '759 patent is titled System and Method of Managing Clock Speed in an Electronic Device. Ex. 1001, code (54). The patent describes a method of monitoring a plurality of master devices coupled to a bus, receiving an input from a master device that is a request to increase the bus clock frequency, and increasing the bus clock frequency in response to the request. *Id.* at code (57).

B. CHALLENGED CLAIMS

Challenged claim 1 is reproduced below:

1. A method, comprising:

monitoring a plurality of master devices coupled to a bus;

receiving a request, from a first master device of the plurality of master devices, to change a clock frequency of a high-speed clock, the request sent from the first master device in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to loading of the first master device as measured within a predefined time interval; and

in response to receiving the request from the first master device:

providing the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus; and

providing the clock frequency of the high-speed clock as an output to control a clock frequency of the bus.

Ex. 1001, 7:66–8:15. Claims 14 and 18 are independent and recite limitations similar to claim 1. *Id.* at 8:50–9:4, 9:19–40. The other challenged claims depend from one of the independent claims.

C. Prior Art and Asserted Grounds

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 14, 17	103	Shaffer[2], Lint[3]
18, 21, 22, 24	103	Shaffer, Lint, Kiriake[4]
1, 14, 17	103	Chen[5], Terrell[6]
18, 21, 22, 24	103	Chen, Terrell, Kiriake

Pet. 7. Petitioner relies also on the Declarations of Dr. Bruce Jacob. Exs. 1002, 1046.

II. ANALYSIS

Our Institution Decision addressed Petitioner's contentions and Patent Owner's challenges to those contentions. *See generally* Inst. We need not repeat that analysis here. In the Director's Decision, she noted that "a compelling-merits challenge is a higher standard than the reasonable likelihood required for the institution of an IPR under 35 U.S.C. § 314(a)."

[2] US 6,298,448 B1, issued Oct. 2, 2001 (Ex. 1005).
[3] US 7,360,103 B2, issued Apr. 15, 2008 (Ex. 1006).
[4] US 2003/0159080 A1, published Aug. 21, 2003 (Ex. 1028).
[5] US 5,838,995, issued Nov. 17, 1998 (Ex. 1003).
[6] US 2004/0098631 A1, published May 20, 2004 (Ex. 1004).

Director Remand at 49. And she further clarified that a compelling-merits challenge requires concluding that it is "highly likely that the petitioner would prevail with respect to at least one challenged claim." *Id.*

A. UNPATENTABILITY GROUNDS INCLUDING SHAFFER AND LINT

Petitioner relies on Schaffer for most limitations of claim 1, further relying on Lint to support that a "predefined change in performance is due to loading of the first master device as measured within a predefined time interval." Pet. 22–31. Petitioner first asserts that Shaffer teaches that limitation by disclosing that "the CPU 20 operates at a lower speed when the OS 32 determines that no processing is occurring or has not occurred for a predetermined amount of time." *Id.* at 27 (quoting Ex. 1005, 4:6–8). Petitioner relies on Lint as an alternative to Shaffer's teachings in that regard, submitting that Lint discloses "changing the 'performance state . . . based in part on the data representing the average performance over the previous period of time.'" *Id.* (quoting Ex. 1006, 3:1–7). Petitioner reasons that Shaffer describes a "CPU utilization percentage" and that Lint discloses a way of calculating that percentage that would allow Shaffer's system "to better interface with processor chips featuring hardware coordination of [performance]-states" by saving power, and that doing so would amount to nothing more than using a known technique to improve similar devices in the same way. *Id.* at 27–30 (citing Ex. 1006, 3:2–7, 2:33; Ex. 1002 ¶¶ 208–226).

Patent Owner contested Petitioner's showing as to the claimed master devices. Prelim. Resp. 31–40. In one aspect, Patent Owner challenged whether Shaffer's memory controller and bus controller could be master devices within the challenged claims. *Id.* at 31–37. We did not find it

necessary to determine whether Petitioner's contentions regarding the memory controller and bus controller justified institution. Inst. 20. Based solely on Petitioner's memory-controller and bus-controller contentions, we would not conclude the Petition presented a compelling-merits challenge.

Petitioner, however, also relied on Shaffer's multiple-CPU embodiment as disclosing a plurality of master devices. Pet. 23. Although Patent Owner challenged whether Shaffer adequately discloses multiple CPUs as master devices (Prelim. Resp. 37–39), we did not agree. Inst. 19–20.

Evaluating the parties' multiple-CPU contentions under the compelling-merits standard, we conclude the record at institution meets that standard. In particular, Shaffer states that, "in a multiprocessor system, . . . a single clock module 50 may drive all the processor clocks." Ex. 1005, 6:2–5. That disclosure supports the principle that the CPUs operate on the same bus. While Patent Owner argued that Shaffer's multiple CPUs would not necessarily act as master devices, would not necessarily connect to the same bus, and would not necessarily each request a speed change (Prelim. Resp. 37–39), those arguments did not undermine the Petition's showing, as further explained below. *See* Inst. 19–20.

As to requesting a speed change, Patent Owner did not seek a construction for "master device" that would require any master device be capable of requesting a speed change. *See* Prelim. Resp. 37–39. Thus, Patent Owner's assertion that Shaffer's multiple CPUs are not master devices because they do not request a speed change was not persuasive. As to connecting to the same bus or acting as master devices, the Petition asserted facts supporting that Shaffer's multiple CPUs would share a bus and

therefore act as master devices. Pet. 23 (citing Ex. 1002 ¶¶ 229–233). Although Patent Owner challenged whether Shaffer's disclosures support Petitioner's asserted facts, Patent Owner did not substantively address statements by Petitioner's expert declarant, and instead only challenged the declaration as hearsay or improperly incorporated argument. *See* Prelim. Resp. 39.

We conclude that the expert testimony relied on in the Petition (Ex. 1002 ¶¶ 231–233), if unrebutted at trial, would plainly lead to a conclusion of unpatentability based on Shaffer's multiple CPUs. *See* Memorandum at 4. That testimony supports the aspects of Petitioner's contentions that were challenged by Patent Owner, and we conclude that testimony presents logical, supported assertions, rooted in Shaffer's disclosures. In particular, Dr. Jacob's testimony asserts that Shaffer's multiple CPUs would operate on the shared "system bus," depicted with shared-bus organization, and using a single clock module. Ex. 1002 ¶¶ 231–232 (citing Ex. 1005, 6:2–5, Fig. 1).

Patent Owner further challenged Petitioner's showing as to an "output to control a clock frequency of the bus." Prelim. Resp. 40–49. In Patent Owner's view, Petitioner relied on different buses in Shaffer, thus failing to show an output to the singular claimed bus. *Id.* Patent Owner's argument in this regard was not persuasive, as it relied on narrowly reading Shaffer and attempted to restrict Shaffer's teachings to one disclosed embodiment. Inst. 20–21. Viewing the evidence under the compelling-merits standard, we conclude that it was highly likely Petitioner would prevail regarding the "output to control a clock frequency of the bus," based on Shaffer's plain disclosures.

For a number of limitations, Patent Owner's Preliminary Response did not challenge Petitioner's assertions regarding Shaffer and Lint. Our review of those limitations indicated that they supported institution (*see* Inst. 21), and upon further review of the record before institution, we conclude that Petitioner's arguments and evidence for these limitations, if unrebutted at trial, would plainly lead to a conclusion of unpatentability.

Patent Owner argued that objective indicia of nonobviousness supported a conclusion of no unpatentability for the '759 patent. Prelim. Resp. 69–71. We determined in the Institution Decision that such arguments presented a factual issue for trial. Inst. 21. At least because Patent Owner's assertions in its Preliminary Response did not address a required element of objective indicia—a nexus with the challenged claims—Patent Owner's assertions of objective indicia do not call into question our view of Petitioner's case-in-chief as having presented a compelling, meritorious challenge prior to institution.

B. Unpatentability Grounds Including Chen and Terrell

Petitioner relies on Chen for most limitations of claim 1, submitting that Terrell additionally teaches requesting a clock speed change "in response to a predefined change in performance of the first master device" and that the predefined change "is due to loading of the first master device as measured within a predefined time interval." Pet. 40–49. Petitioner asserts it would have been obvious to use Terrell's teachings with Chen to adjust Chen's clock speed "based on 'how many clock cycles are being used by each processing element'" because "[r]educing clock speed was a well-known technique for reducing power consumption." Pet. 44 (quoting Ex. 1004 ¶ 26; citing Ex. 1002 ¶¶ 126–142, 145).

Patent Owner contested Petitioner's showing as to whether Chen discloses "providing the clock frequency . . . as an output to control a clock frequency of a second master device." Prelim. Resp. 50–56. In particular, Patent Owner challenged whether Chen's clock controller controlled the frequency of both the bus and multiple master devices on the bus. *Id.*

In this regard, Petitioner relies on Chen's statements that "control logic in the bridge chip causes the higher frequency clock in the bridge chip to be activated such that the host bridge, bus and I/O device are all then operating at the higher frequency" (Ex. 1003, 2:8–14), and "[c]lock gate circuit 24 causes the frequency of bus 40 to be dynamically changed (gated) by transmitting the appropriate device unique clock lines 27." *Id.* at 3:20–22. Because Chen's "unique clock lines 27" are specific to each bus device, we reasoned that those lines control the devices' frequencies. Inst. 25–26. Patent Owner's argument contradicted Chen's plain language and therefore we conclude that Petitioner's assertions, if unrebutted at trial, would plainly lead to a conclusion of unpatentability. That is, we determine the record prior to institution shows that it was highly likely Petitioner would prevail because its contentions were supported by the prior art's disclosures even without supporting expert testimony.

Patent Owner also contested Petitioner's assertions that skilled artisans would have combined Chen and Terrell. Prelim. Resp. 56–69. Specifically, Patent Owner argued that Chen and Terrell have competing interests—Chen in running its bus clock as fast as possible, to accommodate high-speed devices, and Terrell in reducing its clock to the minimum possible speed, to save power. *Id.* at 58–59.

In the Institution Decision, we concluded that Petitioner's expert, Dr. Jacob, adequately explained how a skilled artisan would view the two references as compatible and understand the benefit of combining them. Inst. 27 (citing Ex. 1002 ¶ 136). Petitioner's contentions, as supported by Dr. Jacob, if unrebutted at trial, would plainly lead to a conclusion of unpatentability because his testimony logically and fully explains how the combination would integrate the two references' teachings and offer a benefit. Ex. 1002 ¶¶ 136–145.

Patent Owner argued also that skilled artisans had no reason to look beyond Chen because doing so would increase a system's complexity. Prelim. Resp. 60. As noted in the Institution Decision, that argument failed to apply the applicable standard for obviousness and therefore was not persuasive. Inst. 28. At most, a conclusion that increased complexity would dissuade a skilled artisan from making the combination would require evidence that rebutted Petitioner's showing, which evidence was lacking prior to institution. Thus, Patent Owner's arguments did not undermine the strength of Petitioner's case at institution.

For a number of limitations, Patent Owner's Preliminary Response did not challenge Petitioner's assertions regarding Chen and Terrell. Our review of those limitations indicated that they supported institution (*see* Inst. 29), and upon further review of the record before institution, we conclude that Petitioner's arguments and evidence for these limitations, if unrebutted at trial, would plainly lead to a conclusion of unpatentability.

Considering Patent Owner's arguments against institution and supporting evidence, we conclude it was highly likely Petitioner would

prevail with unpatentability of at least one challenged claim over Chen and Terrell.

III. CONCLUSION

We have reviewed the record prior to institution and considered whether the Petition presents a compelling, meritorious challenge. For the reasons discussed above, we conclude the Petition and supporting evidence, if unrebutted at trial, would plainly lead to a conclusion that one or more challenged claims are unpatentable. Balanced against Patent Owner's arguments and evidence against institution, the record prior to institution supports that it was highly likely that Petitioner would prevail with respect to at least one challenged claim.

IV. ORDER

Accordingly, it is

ORDERED that the record before the Board prior to institution in this proceeding indicates that the Petition presents a compelling, meritorious challenge.

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