U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

CLASSIFICATION ORDER 1872

DATE November 06, 2007

PROJECT NO. E 6508

The following classification changes will be effected by this order:

	Class	Subclass	Art Unit	Ex'r Search Room No.
Abolished:	**365**	49, 189.01, 210, 233	2827	0S001
Established:	**365**	49.1, 49.11-49.13, 49.15-49.18, 189.011, 189.14-189.19, 189.2, 210.1, 210.11-210.15, 233.1, 233.11-233.19	2827	0S001
Indent Changes:	**365**	207, 208, 209		
Title Changes:	**365**	50		

The following classes are also impacted by this order:
307, 327, 345, 359, 361, 369, 370, 375, 711

A. CLASSIFICATION MANUAL CHANGES

B. LISTING OF PRINCIPAL SOURCE OF ESTABLISHED AND DISPOSITION OF ABOLISHED PAGES

C. CHANGES TO THE U.S.-I.P.C. CONCORDANCE

D. DEFINITION CHANGES AND NEW OR ADDITIONAL DEFINITIONS

CLASSIFICATION ORDER 1872
NOVEMBER 06, 2007
PROJECT NO. E-6508

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1 MAGNETIC BUBBLES
2 .Disposition of elements
3 ..Lattice
4 .Decoder
5 .Logic
6 .Rotating field circuits
7 .Detectors
8 ..Magnetoresistive
9 ..Hall effect
10 ..Optical
11 .Generators
12 ..By splitting
13 .Plural interacting paths
14 ..Closed loop
15 ...Major-minor
16 ..With switch at interacting point
17 ...Idler switch
18 ..Boundary
19 .Conductor propagation
20 ..Including A.C. signal
21 ..Three phase signals
22 .One's and zero's
23 .Plural direction propagation
24 ..Nonsequential
25 .Velocity
26 ..Turns
27 .Bias
28 ..Variable
29 .Strip domain
30 .In-plane field (nonrotating)
31 .Different size bubbles
32 .Multiple magnetic layer
33 .Magnetic storage material
34 ..Amorphous
35 .Guide structure
36 ..Ion implantation
37 ..Slots or rails
38 ..Zigzag
39 ..Overlays
40 ...On opposite sides of storage medium
41 ...Dots
42 ...Wedges
43 ...Chevrons
44 ...Rectangular bars
185.01 FLOATING GATE
185.02 .Disturbance control
185.03 .Multiple values (e.g., analog)
185.04 .Data security
185.05 .Particular connection
185.06 ..Segregated columns
185.07 ..Cross-coupled cell
185.08 ..With volatile signal storage device
185.09 ..Error correction (e.g., redundancy, endurance)
185.1 ..Extended floating gate
185.11 ..Bank or block architecture
185.12 ...Parallel row lines (e.g., page mode)
185.13 ...Global word or bit lines
185.14 ..Program gate
185.15 ...Weak inversion injection
185.16 ..Virtual ground
185.17 ..Logic connection (e.g., NAND string)
185.18 .Particular biasing
185.19 ..Multiple pulses (e.g., ramp)
185.2 ..Reference signal (e.g., dummy cell)
185.21 ...Sensing circuitry (e.g., current mirror)
185.22 ...Verify signal
185.23 ..Drive circuitry (e.g., word line driver)
185.24 ..Threshold setting (e.g., conditioning)
185.25 ..Line charging (e.g., precharge. discharge, refresh)
185.26 ..Floating electrode (e.g., source. control gate, drain)
185.27 ..substrate bias
185.28 ..Tunnel programming
185.29 ..Erase
185.3 ...Over erasure
185.31 ...Nonsubstrate discharge
185.32 ....Radiation erasure
185.33 ...Flash
45 ANALOG STORAGE SYSTEMS
46 .Resistive
47 .Thermoplastic
48 .Magnetic
* 49.1 ASSOCIATIVE MEMORIES (Content Addressable Memory-CAM)
* 49.11 .Flip-Flop
* 49.12 .Capacitor cell
* 49.13 .Ferroelectric cell
# 50 .Magnetic cell
* 49.15 .Auxiliary lines
* 49.16 .Segmented/Partitioned of cells
* 49.17 .Compare/Search/Match circuit
* 49.18 .Priority encoders
51 FORMAT OR DISPOSITION OF ELEMENTS
52 HARDWARE FOR STORAGE ELEMENTS
53 .Shields
54 .Ground plane
55 .Magnetic
56 ..spacers
57 ..Keeper
58 ..Slot
59 ..Embedded conductor
60 ..Air gap
61 ..Hairpin conductor
62 ..Permanent magnet
63 INTERCONNECTION ARRANGEMENTS
64 .Optical
65 .Ferroelectric
66 .Magnetic
67 ..Plural diagonal
68 ..Tree
69 ..Crossover
70 ..Woven
71 .Negative resistance
72 .Transistors or diodes
73 RECIRCULATION STORES
74 .Magnetic
75 .Stepwise
76 .Delay lines
77 .Plural paths
78 PLURAL SHIFT REGISTER MEMORY DEVICES

READ/WRITE CIRCUIT
189.08 .Including specified plural element logic arrangement
189.09 .Including reference or bias voltage generator
189.11 .Including level shift or pull-up circuit
189.12 .With shift register
190 .For complementary information
191 .Signals
192 ..Radio frequency
193 ..Strobe
194 ..Delay
195 ..Inhibit
196 ...Sense/inhibit
197 ..Microwave
198 ..Transmission
199 ..coincident A.C. signal with pulse
200 .Bad bit
201 .Testing
202 .Complementing/balancing
203 .Precharge
204 .Accelerating charge or discharge
205 .Flip-flop used for sensing
206 .Noise suppression
@ 207 .Differential sensing
@ 208 ..Semiconductors
@ 209 ..Magnetic
* 210.1 ..Reference or dummy element
* 210.11 ...Compensate signal
* 210.12 ...Voltage setting
* 210.13 ...Common bit line
* 210.14 ...Plural elements per reference cell
* 210.15 ...Structural compoment of a reference cell
211 ..Temperature compensation
212 ...Semiconductor
213 ...Magnetic
214 ..Particular wiring
215 .Optical
216 ..Holographic
217 .Electron beam
218 .Erase
219 .SiPo/PiSo
220 .Parallel read/write
221 .Serial read/write
222 .Data refresh
223 .Bridge
224 .Eddy current
225 .Minor loop
225.5 .Including magnetic element
225.6 .Having bipolar circuit element
225.7 .Having fuse element
226 POWERING
227 .Conservation of power
228 .Data preservation
229 ..standby power
230.01 ADDRESSING
230.02 .Multiplexing
230.03 .Plural blocks or hanks
230.04 ..Alternate addressing (e.g., even/odd)
230.05 .Multiple port access
230.06 .Particular decoder or driver circuit
230.07 ..Including magnetic element
230.08 .Including particular address buffer or latch circuit arrangement
230.09 .Combined random and sequential addressing
231 .Using selective matrix
232 ..Magnetic
* 233.1 .Sync/clocking
* 233.11 ..Plural clock signals
* 233.12 ..External clock signal modification
* 233.13 ..DDR (double data rate) memory
* 233.14 ..Initiating signal
* 233.15 ..standby signal
* 233.16 ..Write mode signal only
* 233.17 ..Read mode signal only
* 233.18 ..Burst mode signal
* 233.19 ..Common read and write mode signal
233.5 ..Transition detection
234 .Optical
235 ..Page memories
236 .Counting
237 .Electron beam
238 .Cartesian memories
238.5 .Byte or page addressing
239 .Sequential
240 ..Using shift register
241 ..Detectors
242 .Current Steering
243 ..Diode
243.5 .Including magnetic element
244 MISCELLANEOUS
****
FOREIGN ART COLLECTION
****
FOR 000 CLASS-RELATED FOREIGN DOCUMENTS

NOVEMBER 6, 2007

PROJECT E-6508

SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

generated by: Data Control Division

New Classification	Number Of ORs	Source Classification	Number Of ORs
257/206	1	365/189.01	469
327/175	1	365/233	1147
335/207	1	365/210	267
365/104	1	365/189.01	469
	1	365/210	267
365/120	1	365/189.01	469
365/145	1	365/210	267
	1	365/233	1147
365/148	1	365/210	267
365/149	14	365/210	267
	2	365/233	1147
365/154	9	365/233	1147
365/158	1	365/189.01	469
	4	365/210	267
	1	365/233	1147
365/171	2	365/210	267
365/174	1	365/210	267
365/175	1	365/210	267
365/185.01	1	365/189.01	469
	1	365/210	267
365/185.05	1	365/233	1147
365/185.06	1	365/189.01	469
365/185.13	1	365/189.01	469
	1	365/210	267
365/185.14	1	365/189.01	469
365/185.17	15	365/233	1147
365/185.18	1	365/189.01	469
365/185.2	5	365/210	267
365/185.21	1	365/210	267
	1	365/233	1147
365/185.23	1	365/189.01	469
365/185.24	1	365/210	267
365/185.26	1	365/210	267
365/185.28	1	365/233	1147
365/185.29	1	365/233	1147
365/185.33	1	365/210	267
365/189.011	28	365/189.01	469
	1	365/210	267
	4	365/233	1147
365/189.02	5	365/189.01	469
	1	365/210	267

SOURCE CLASSIFICATION(S) OF PATENTS
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by: Data Control Division

New Classification	Number Of ORs	Source Classification	Number Of ORs
	16	365/233	1147
365/189.03	18	365/189.01	469
	1	365/210	267
365/189.03	3	365/233	1147
365/189.04	12	365/189.01	469
	2	365/233	1147
365/189.05	3	365/189.01	469
	1	365/210	267
	22	365/233	1147
365/189.06	1	365/49	789
365/189.07	6	365/189.01	469
	5	365/210	267
	10	365/233	1147
365/189.08	1	365/189.01	469
	1	365/210	267
	5	365/233	1147
365/189.09	4	365/189.01	469
	8	365/210	267
	4	365/233	1147
365/189.11	2	365/189.01	469
	1	365/210	267
365/189.12	1	365/210	267
365/189.14	77	365/189.01	469
	1	365/210	267
	29	365/233	1147
365/189.15	128	365/189.01	469
	9	365/210	267
	49	365/233	1147
365/189.16	99	365/189.01	469
	1	365/210	267
	17	365/233	1147
365/189.17	13	365/189.01	469
	7	365/233	1147
365/189.18	19	365/189.01	469
	3	365/233	1147
365/189.19	6	365/189.01	469
	1	365/233	1147
365/189.2	3	365/189.01	469
	1	365/233	1147
365/190	1	365/189.01	469

NOVEMBER 6, 2007

PROJECT E-6508

SOURCE CLASSIFICATION(S) OF PATENTS IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by: Data Control Division

New Classification	Number Of ORs	Source Classification	Number Of ORs
	6	365/210	267
365/191	1	365/210	267
	5	365/233	1147
365/193	10	365/233	1147
365/194	1	365/210	267
	32	365/233	1147
365/195	1	365/189.01	469
365/195	1	365/233	1147
365/196	1	365/189.01	469
365/200	2	365/189.01	469
	1	365/210	267
365/201	3	365/189.01	469
	1	365/210	267
	1	365/233	1147
365/203	1	365/189.01	469
	5	365/210	267
	1	365/233	1147
365/205	2	365/189.01	469
	12	365/210	267
365/207	2	365/189.01	469
	17	365/210	267
365/208	1	365/233	1147
365/210.1	91	365/210	267
	2	365/233	1147
365/210.11	2	365/210	267
	1	365/233	1147
365/210.12	34	365/210	267
365/210.13	1	365/189.01	469
	8	365/210	267
365/210.14	1	365/189.01	469
	3	365/210	267
365/210.15	7	365/210	267
365/218	1	365/233	1147
365/221	1	365/189.01	469
	1	365/233	1147
365/222	1	365/233	1147
365/225.7	1	365/210	267
365/226	1	365/189.01	469
	1	365/233	1147

SOURCE CLASSIFICATION(S) OF PATENTS IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by: Data Control Division

New Classification	Number Of ORs	Source Classification	Number Of ORs
365/227	1	365/233	1147
365/230.01	8	365/233	1147
	1	365/49	789
365/230.02	4	365/233	1147
365/230.03	1	365/189.01	469
	20	365/233	1147
365/230.04	2	365/189.01	469
	4	365/233	1147
365/230.06	6	365/189.01	469
	4	365/210	267
	11	365/233	1147
365/230.08	1	365/189.01	469
365/230.08	2	365/233	1147
365/230.09	1	365/189.01	469
	2	365/233	1147
365/233.1	1	365/189.01	469
	392	365/233	1147
365/233.11	1	365/189.01	469
	105	365/233	1147
365/233.12	74	365/233	1147
365/233.13	39	365/233	1147
365/233.14	83	365/233	1147
365/233.15	1	365/189.01	469
	10	365/233	1147
365/233.16	54	365/233	1147
365/233.17	37	365/233	1147
365/233.18	2	365/189.01	469
	14	365/233	1147
365/233.19	9	365/233	1147
365/233.5	3	365/233	1147
365/236	1	365/233	1147
365/45	1	365/49	789
365/49.1	1	365/210	267
	214	365/49	789
365/49.11	74	365/49	789
365/49.12	31	365/49	789
365/49.13	4	365/49	789
365/49.15	109	365/49	789

SOURCE CLASSIFICATION (S) OF PAGES
IN NEWLY ESTABLISHED SUBCLASSES REPORT

Generated by: Data Control Division

New Classification	Number Of ORs	Source Classification	Number Of ORs
365/49.16	24	365/49	789
365/49.17	271	365/49	789
365/49.18	45	365/49	789
365/50	2	365/49	789
365/51	1	365/210	267
	4	365/233	1147
365/63	1	365/210	267
	3	365/233	1147
	1	365/49	789
365/94	1	365/189.01	469
	1	365/210	267
	2	365/233	1147
711/102	1	365/210	267
711/105	4	365/49	789
711/108	6	365/49	789
711/125	1	365/49	789
711/167	1	365/233	1147
712/208	1	365/189.01	469

PROJECT E-6508

DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by: Data Control Division

Source Classification	Number Of ORs	New Classification	Number Of ORs
365/189.01	469	257/206	1
		365/104	1
		365/120	1
		365/158	1
		365/185.01	1
		365/185.06	1
		365/185.13	1
		365/185.14	1
		365/185.18	1
		365/185.23	1
		365/189.011	28
		365/189.02	5
		365/189.03	18
		365/189.04	12
		365/189.05	3
		365/189.07	6
		365/189.08	1
		365/189.09	4
		365/189.11	2
		365/189.14	77
		365/189.15	128
		365/189.16	99
		365/189.17	13
		365/189.18	19
		365/189.19	6
		365/189.2	3
		365/190	1
		365/195	1
		365/196	1
		365/200	2
		365/201	3
		365/203	1
		365/205	2
		365/207	2
		365/210.13	1
		365/210.14	1
		365/221	1
		365/226	1
		365/230.03	1
		365/230.04	2
		365/230.06	6

PROJECT E-6508

DISPOSITION CLASSIFICATION(S) OF PATENTS FROM ABOLISHED SUBCLASSES REPORT

Generated by: Data Control Division

Source Classification	Number Of ORs	New Classification	Number Of ORs
365/230.08	1		
		365/230.09	1
		365/233.1	1
		365/233.11	1
		365/233.15	1
365/189.01	469	365/233.18	2
		365/94	1
		712/208	1
365/210	267	335/207	1
		365/104	1
		365/145	1
		365/148	1
		365/149	14
		365/158	4
		365/171	2
		365/174	1
		365/175	1
		365/185.01	1
		365/185.13	1
		365/185.2	5
		365/185.21	1
		365/185.24	1
		365/185.26	1
		365/185.33	1
		365/189.011	1
		365/189.02	1
		365/189.03	1
		365/189.05	1
		365/189.07	5
		365/189.08	1
		365/189.09	8
		365/189.11	1
		365/189.12	1
		365/189.14	1
		365/189.15	9
		365/189.16	1
		365/190	6
		365/191	1
		365/194	1

PROJECT E-6508

DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT

Generated by: Data Control Division

Source Classification	Number Of ORs	New Classification	Number Of ORs
		365/200	1
		365/201	1
		365/203	5
		365/205	12
		365/207	17
		365/210.1	91
		365/210.11	2
		365/210.12	34
		365/210.13	8
		365/210.14	3
		365/210.15	7
		365/225.7	1
365/210	267	365/230.06	4
		365/49.1	1
		365/51	1
		365/63	1
		365/94	1
		711/102	1
365/233	1147	327/175	1
		365/145	1
		365/149	2
		365/154	9
		365/158	1
		365/185.05	1
		365/185.17	15
		365/185.21	1
		365/185.28	1
		365/185.29	1
		365/189.011	4
		365/189.02	16
		365/189.03	3
		365/189.04	2
		365/189.05	22
		365/189.07	10
		365/189.08	5
		365/189.09	4
		365/189.14	29
		365/189.15	49
		365/189.16	17

DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT
PROJECT: E6508

Generated by: Data Control Division

Source Classification	Number Of ORs	New Classification	Number Of ORs
		365/189.17	7
		365/189.18	3
		365/189.19	1
		365/189.2	1
		365/191	5
		365/193	10
		365/194	32
		365/195	1
		365/201	1
		365/203	1
		365/208	1
		365/210.1	2
		365/210.11	1
		365/218	1
		365/221	1
		365/222	1
		365/226	1
		365/227	1
		365/230.01	8
365/233	1147	365/230.02	4
		365/230.03	20
		365/230.04	4
		365/230.06	11
		365/230.08	2
		365/230.09	2
		365/233.1	392
		365/233.11	105
		365/233.12	74
		365/233.13	39
		365/233.14	83
		365/233.15	10
		365/233.16	54
		365/233.17	37
		365/233.18	14
		365/233.19	9
		365/233.5	3
		365/236	1
		365/51	4
		365/63	3
		365/94	2

		711/167	1

DISPOSITION CLASSIFICATION(S) OF PATENTS
FROM ABOLISHED SUBCLASSES REPORT
PROJECT: E6508

Generated by: Data Control Division

Source	Number	New	Number
365/49	789	365/189.06	1
		365/230.01	1
		365/45	1
		365/49.1	214
		365/49.11	74
		365/49.12	31
		365/49.13	4
		365/49.15	109
		365/49.16	24
		365/49.17	271
		365/49.18	45
		365/50	2
		365/63	1
		711/105	4
		711/108	6
		711/125	1

C. CHANGES TO THE USPC-TO-IPC CONCORDANCE

USPC Class	USPC Subclass	IPC Subclass	IPC Notation
365	49.1	G11C	15/00
	49.11	G11C	15/00
	49.12	G11C	15/04
	49.13	G11C	15/00
	50	G11C	15/02
	49.15	G11C	15/00
	49.16	G11C	15/00
	49.17	G11C	15/00
	49.18	G11C	15/00
	189.011	G11C	7/00, 7/22
	189.02	G11C	7/00
	189.03	G11C	7/10
	189.04	G11C	7/00, 7/22
	189.14	G11C	7/00, 7/22
	189.15	G11C	7/00, 7/22
	189.16	G11C	7/00, 7/22
	189.17	G11C	7/10
	189.18	G11C	7/18, 7/00
	189.19	G11C	7/18, 7/00
	189.2	G11C	7/00
	210.1	G11C	7/02
	210.11	G11C	7/02
	210.12	G11C	7/02
	210.13	G11C	7/02
	210.14	G11C	7/02
	210.15	G11C	7/02
	233.1	G11C	8/00
	233.11	G11C	8/18
	233.12	G11C	8/18
	233.13	G11C	8/16
	233.14	G11C	8/00; 8/18
	233.15	G11C	8/00; 8/18
	233.16	G11C	8/00; 8/18
	233.17	G11C	8/00; 8/18
	233.18	G11C	8/00; 8/18
	233.19	G11C	8/00; 8/18

D. CHANGES TO THE DEFINITIONS

CLASS 307 – ELECTRICAL TRANSMISSION OR INTERCONNECTION SYSTEMS

Class Definition: Section II, under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 185.01+ for floating gate memory storage (e.g., flash memory), subclass 73 for recirculation of information in a storage read/write system, subclass 78 for plural shift register memory devices, subclass 80 for magnetic shift register, per se, subclasses 129+ for storage systems using a particular storage element, subclasses 189.01+ for read/write circuits peculiar to a storage and retrieval system, and subclass 230 for addressing circuits peculiar to a storage and retrieval system.

Insert:

365, Static Information Storage and Retrieval, subclasses 185.01+ for floating gate memory storage (e.g., flash memory), subclass 73 for recirculation of information in a storage read/write system, subclass 78 for plural shift register memory devices, subclass 80 for magnetic shift register, per se, subclasses 129+ for storage systems using a particular storage element, subclass 189.011 for read/write circuits peculiar to a storage and retrieval system, and subclass 230 for addressing circuits peculiar to a storage and retrieval system.

D. CHANGES TO THE DEFINITIONS

CLASS 327 – MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR DEVICES, CIRCUITS, AND SYSTEMS

Class Definition: Section IV, under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 73+ for recirculation of information in a storage read/write system, subclass 78 for plural shift register memory devices, subclasses 80+ for magnetic shift register, per se, subclasses 129+ for storage systems using a particular storage element, subclasses 189.01+ for read/write circuits peculiar to a storage and retrieval system, and subclasses 230.01+ for addressing circuits peculiar to a storage and retrieval system. (Also see "Charge Coupled Devices" above).

Insert:

365, Static Information Storage and Retrieval, subclasses 73+ for recirculation of information in a storage read/write system, subclass 78 for plural shift register memory devices, subclasses 80+ for magnetic shift register, per se, subclasses 129+ for storage systems using a particular storage element, subclass 189.011 for read/write circuits peculiar to a storage and retrieval system, and subclasses 230.01+ for addressing circuits peculiar to a storage and retrieval system. (Also see "Charge Coupled Devices" above).

Subclass 51: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01+ for networks including the inserting, extracting, or handling of information signals using the functions of "write", "read-out", "erase", etc., subclasses 185.01+ for floating gate memory storage (e.g., flash memory); subclasses 189.01+ for the static storage and retrieval of information coupled with the functions of "write", "read-out", "erase", etc., wherein voltage amplitude is sensed.

Insert:

365, Static Information Storage and Retrieval, subclasses 207- 210.15 for the static storage and retrieval of information coupled with the

D. CHANGES TO THE DEFINITIONS

functions of "write", "read-out", "erase", etc., wherein voltage amplitude is sensed.

D. CHANGES TO THE DEFINITIONS

CLASS 345 – COMPUTER GRAPHICS PROCESSING AND SELECTIVE VISUAL DISPLAY SYSTEMS

Subclass 519: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, appropriate subclasses, in particular subclasses 189.01+ and 230.01+ for read/write and addressing circuitry for a semiconductor structure device

Insert:

365, Static Information Storage and Retrieval, appropriate subclasses, in particular subclasses 189.011 and 230.01+ for read/write and addressing circuitry for a semiconductor structure device.

Subclass 530: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, various subclasses for static memory devices including internal elements of the memory, particularly subclasses 189.01 through 189.12 for read/write circuits and subclasses 230.01-230.09 for addressing of addressable, static single storage elements or plural elements; subclass 189.05 for buffering or latching data being read from or written to memory; subclass 189.08 for logic devices in combination with memory systems; subclasses 200 and 201 for testing of memory systems; and subclass 230.08 for buffering and latching address data being employed to access memory.

Insert:

365, Static Information Storage and Retrieval, various subclasses for static memory devices including internal elements of the memory, particularly subclasses 189.011 through 189.19 for read/write circuits and subclasses 230.01-230.09 for addressing of addressable, static single storage elements or plural elements; subclass 189.05 for buffering or latching data being read from or written to memory; subclass 189.08 for logic devices in combination with memory systems; subclasses 200 and 201 for testing of memory systems; and subclass 230.08 for buffering and latching address data being employed to access memory.

D. CHANGES TO THE DEFINITIONS

Subclass 531: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses, 189.01-189.12 for read/write circuit.

Insert

365, Static Information Storage and Retrieval, subclasses, 189.01 through 189.19 for read/write circuit.

D. CHANGES TO THE DEFINITIONS

CLASS 359 – OPTICAL: SYSTEMS AND ELEMENTS

Subclass 11: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclass 49 for associative holographic memories.

Insert:

365, Static Information Storage and Retrieval, subclass 49.1 for associative holographic memories.

D. CHANGES TO THE DEFINITIONS

CLASS 361 – ELECTRICITY: ELECTRICAL SYSTEMS AND DEVICES

Subclass 684: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 1+ for magnetic bubbles, per se; subclasses 185.01+ for floating gate memory storage (e.g., flash memory); subclasses 45+ for analog storage systems, per se; subclasses 49+ for associative memories, per se; and subclasses 94+ for read only systems, per se.

Insert:

365, Static Information Storage and Retrieval, subclasses 1+ for magnetic bubbles, per se; subclasses 185.01+ for floating gate memory storage (e.g., flash memory); subclasses 45+ for analog storage systems, per se; subclasses 49.1 through 50 for associative memories, per se; and subclasses 94+ for read only systems, per se.

D. CHANGES TO THE DEFINITIONS

CLASS 365 – STATIC INFORMATION STORAGE AND RETRIEVAL

Definitions Abolished

Subclasses

49, 189.01, 210, 233

Definitions Modified

Class Definition: Section III, under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

49, through 243.5, digital storage systems, for devices where the information is discrete.

Insert:

49.1, through 243.5, digital storage systems, for devices where the information is discrete.

Subclass 50: In the subclass definition

Delete:

50 This subclass is indented under subclass 49. Subject matter where the associative memories storage elements are magnetic.

Insert:

50 Magnetic cell:
Subject matter under subclass 49.1 wherein the storage element changes a storage state when a magnetic field is applied.

D. CHANGES TO THE DEFINITIONS

Subclass 63: Under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

189.01+, for reading or writing information from or into a static memory device.

Insert:

189.011, for reading or writing information from or into a static memory device

Subclass 185.2: Under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

210, for noise suppression by differential sensing using a reference or dummy elements.

Insert:

210.1, for noise suppression by differential sensing using a reference or dummy elements.

Subclass 189.02: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter which includes the transmission of plural signals over a single signal path.

Insert:

This subclass is indented under subclass 189.011. Subject matter which includes the transmission of plural signals over a single signal path.

Subclass 189.03: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter which has a terminal connecting the memory to a data handling circuit and another diverse circuit.

D. CHANGES TO THE DEFINITIONS

Insert:

This subclass is indented under subclass 189.011. Subject matter which has a terminal connecting the memory to a data handling circuit and another diverse circuit.

Subclass 189.04: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including circuitry for performing multiple operations (e.g., storing information in and retrieving information from the memory) at the same time.

Insert:

This subclass is indented under subclass 189.011. Subject matter including circuitry for performing multiple operations (e.g., storing information in and retrieving information from the memory) at the same time.

Subclass 189.05: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a specific detail of a temporary storage circuit for a data signal.

Insert:

This subclass is indented under subclass 189.011. Subject matter including a specific detail of a temporary storage circuit for a data signal.

Subclass 189.06: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including circuitry for limiting the variation of a signal (e.g., voltage) in order to keep such variation at a predetermined level.

Insert:

This subclass is indented under subclass 189.011. Subject matter including circuitry for limiting the variation of a signal (e.g., voltage) in order to keep such variation at a predetermined level.

D. CHANGES TO THE DEFINITIONS

Subclass 189.07: In the subclass definition

Delete :

This subclass is indented under subclass 189.01. Subject matter including circuitry to compare plural signal in order to control an operation of the system on a data signal.

Insert:

This subclass is indented under subclass 189.011. Subject matter including circuitry to compare plural signal in order to control an operation of the system on a data signal.

Under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

49, for a comparator in a content addressable memory.

Insert:

49.17, for a comparator in a content addressable memory.

Subclass 189.08: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter describing the configuration of multiple logic devices which handle the information signal.

Insert:

This subclass is indented under subclass 189.011. Subject matter describing the configuration of multiple logic devices which handle the information signal.

Subclass 189.09: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a particular voltage or bias source.

Insert:

This subclass is indented under subclass 189.011. Subject matter including a particular voltage or bias source.

D. CHANGES TO THE DEFINITIONS

Under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

210, for an element used to generate reference voltage for a sense amplifier.

Insert:

210.1-210.15, for an element used to generate reference voltage for a sense amplifier.

Subclass 189.11 : In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a circuit element which makes an adjustment in the voltage level of an information signal to enhance driving capability.

Insert:

This subclass is indented under subclass 189.011. Subject matter including a circuit element which makes an adjustment in the voltage level of an information signal to enhance driving capability.

Subclass 189.12: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a circuit which sequentially shifts the data information signal between one element and another in a memory array in a serial manner.

Insert:

This subclass is indented under subclass 189.011. Subject matter including a circuit which sequentially shifts the data information signal between one element and another in a memory array in a serial manner.

Subclass 190: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein the read/write circuit is used with a memory cell containing complementary information.

D. CHANGES TO THE DEFINITIONS

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein the read/write circuit is used with a memory cell containing complementary information.

Subclass 191: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter where particular signals are used for writing, maintaining, or reading information.

Insert:

This subclass is indented under subclass 189.011. Subject matter where particular signals are used for writing, maintaining, or reading information.

Subclass 200: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which erroneous, defective, or partially defective storage locations are used to store information.

Insert:

This subclass is indented under subclass 189.011. Subject matter in which erroneous, defective, or partially defective storage locations are used to store information.

Subclass 201: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including the specifics of the memory which are tested for defects or erroneous information.

Insert:

This subclass is indented under subclass 189.011. Subject matter including the specifics of the memory which are tested for defects or erroneous information.

D. CHANGES TO THE DEFINITIONS

Subclass 202: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which complementing or balancing signals are used in a read/write circuit, e.g., a storage system having an auxiliary storage circuit for complementary signals to be used for noise cancellation.

Insert:

This subclass is indented under subclass 189.011. Subject matter in which complementing or balancing signals are used in a read/write circuit, e.g., a storage system having an auxiliary storage circuit for complementary signals to be used for noise cancellation.

Subclass 203: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein circuit lines or elements are charged (or discharged) to a desired level just prior to reading or writing information.

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein circuit lines or elements are charged (or discharged) to a desired level just prior to reading or writing information.

Subclass 204: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein a circuit senses a charging (or discharging) operation and switches in a parallel path to decrease the charging (or discharging) time.

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein a circuit senses a charging (or discharging) operation and switches in a parallel path to decrease the charging (or discharging) time.

Subclass 205 : In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein the sensing circuit is a flip-flop circuit.

D. CHANGES TO THE DEFINITIONS

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein the sensing circuit is a flip-flop circuit.

Subclass 206: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter having circuits for cancellation or reduction of noise or spurious signals.

Insert:

This subclass is indented under subclass 189.011. Subject matter having circuits for cancellation or reduction of noise or spurious signals.

Subclass 207: In the subclass definition

Delete:

This subclass is indented under subclass 206. Subject matter where the circuit used is of the differential sensing type.

Insert:

This subclass is indented under subclass 189.011. Subject matter includes a circuit for detecting the difference between two voltage or current levels.

Subclass 215: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which the read/write circuit if for an optical storage system.

Insert:

This subclass is indented under subclass 189.011. Subject matter in which the read/write circuit if for an optical storage system.

Subclass 217: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which the read/write circuit is for an electron beam storage system.

D. CHANGES TO THE DEFINITIONS

Insert:

This subclass is indented under subclass 189.011. Subject matter in which the read/write circuit is for an electron beam storage system.

Subclass 218: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which the read/write circuit is or includes an erase circuit for a storage system.

Insert:

This subclass is indented under subclass 189.011. Subject matter in which the read/write circuit is or includes an erase circuit for a storage system.

Subclass 219: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter in which the read/write circuit for memory provides Serial Input with Parallel Output or Parallel Input with Serial Output.

Insert:

This subclass is indented under subclass 189.011. Subject matter in which the read/write circuit for memory provides Serial Input with Parallel Output or Parallel Input with Serial Output.

Subclass 220: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein information is written into a memory in parallel form and read out in parallel form.

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein information is written into a memory in parallel form and read out in parallel form.

Subclass 221: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein information is written into a memory in serial form and read out in serial form.

D. CHANGES TO THE DEFINITIONS

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein information is written into a memory in serial form and read out in serial form.

Subclass 222 : In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein decaying information is read before it becomes unrecognizable, and rewritten in original form, e.g., charge on a capacitor is read before too much has leaked off, then rewritten to a fully charged state.

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein decaying information is read before it becomes unrecognizable, and rewritten in original form, e.g., charge on a capacitor is read before too much has leaked off, then rewritten to a fully charged state.

Subclass 223 : In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter where the sensing circuit is in the form of a bridge circuit.

Insert:

This subclass is indented under subclass 189.011. Subject matter where the sensing circuit is in the form of a bridge circuit.

Subclass 224: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter having circuits containing Eddy currents.

Insert:

This subclass is indented under subclass 189.011. Subject matter having circuits containing Eddy currents.

D. CHANGES TO THE DEFINITIONS

Subclass 225: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter where the read/write circuit results in the operation of a magnetic memory element or any hysteresis loop other than the major loop.

Insert:

This subclass is indented under subclass 189.011. Subject matter where the read/write circuit results in the operation of a magnetic memory element or any hysteresis loop other than the major loop.

Subclass 225.5: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a semiconductor element having plural potential barriers (i.e., junctions).

Insert:

This subclass is indented under subclass 189.011. Subject matter including a semiconductor element having plural potential barriers (i.e., junctions).

Subclass 225.6: In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter including a semiconductor element having plural potential barriers (i.e., junctions).

Insert:

This subclass is indented under subclass 189.011. Subject matter including a semiconductor element having plural potential barriers (i.e., junctions).

Subclass 225.7 : In the subclass definition

Delete:

This subclass is indented under subclass 189.01. Subject matter wherein the circuit includes a circuit element which is selectively melted or disintegrated to make or break an electric circuit to control the operating characteristics of a memory read or write circuit.

Insert:

This subclass is indented under subclass 189.011. Subject matter wherein the circuit includes a circuit element which is selectively melted or disintegrated to

D. CHANGES TO THE DEFINITIONS

make or break an electric circuit to control the operating characteristics of a memory read or write circuit.

Subclass 230.01: Under SEE OR SEARCH THIS CLASS, SUBCLASS

Delete:

189.01+, for the reading or writing of information in a memory system.

Insert:

189.011, for the reading or writing of information in a memory system.

Subclass 233.5: In the subclass definition

Delete:

This subclass is indented under subclass 233. Subject matter which generates a clock or timing signal responsive to a change in an input signal.

Insert:

This subclass is indented under subclass 233.1. Subject matter which generates a clock or timing signal responsive to a change in an input signal.

Definition established

49.1 ASSOCIATIVE MEMORIES (Content Addressable Memory-CAM)

This subclass is indented under the class definition. Subject matter wherein the location of the information is determined by its content rather than by its address.

(1) Note. associative memories are also referred to as content or tag memories.

49.11 Flip-Flop:

Subject matter under subclass 49.1 wherein the storage element is a bistable logic circuit (i.e., one in which information need not be periodically refreshed).

49.12 Capacitor cell:

Subject matter under subclass 49.1 wherein the storage element is a capacitative device (i.e., one in which information need to be periodically refreshed).

49.13 Ferroelectric cell:

Subject matter under subclass 49.1 wherein the storage element is a ferroelectric memory cell.

D. CHANGES TO THE DEFINITIONS

49.15 Auxiliary lines:
Subject matter under subclass 49.1 where a line that carries hit/miss signals (match or missmatch signals) in a content addressable memory (CAM) is used for comparison in addition to the lines that carry the bit lines.

49.16 Segmented/Partitioned of cells:
Subject matter under subclass 49.1 where CAM elements are grouped into segments or partitions.

49.17 Compare/Search/Match circuit:
Subject matter under subclass 49.1 including a circuit for comparison of storage data and search data and outputing match/mismatch (hit/miss) signals.

49.18 Priority encoders:
Subject matter under subclass 49.1 including means to indicate an order of transmission of search data in a content addressable memory (CAM).

189.011 READ/WRITE CIRCUIT:
This subclass is indented under the class definition. Subject matter for inserting, extracting, or handling of an information signal to be stored (write circuit) or retrieved (read circuit).

189.14 Common read and write circuit:
Subject matter under subclass 189.011 including a circuit for controlling both reading and writing of data signal from/to a memory location.

189.15 Particular read circuit:
Subject matter under subclass 189.011 including a circuit for controlling reading of data signal from a memory location.

189.16 Particular write circuit:
Subject matter under subclass 89.011 including a circuit for controlling writing of data signal to a memory location.

189.17 Data transfer circuit:
Subject matter under subclass 189.011 including a circuit that connects between two storage locations (e.g., two memory arrays or memory blocks) for transferring data between them.

189.18 Bidirectional bus:
Subject matter under subclass 189.011 wherein data input/output lines are used for both reading and writing of data.

189.19 Separate read and write bus:
Subject matter under subclass 189.011 wherein each of read and write bus is unidirectional.

D. CHANGES TO THE DEFINITIONS

189.2 Using different memory types:
Subject matter under subclass 189.011 including a bus interface circuit between independent memory types (e.g., DRAM and SRAM).

210.1 Reference or dummy element:
This subclass is indented under subclass 207. Subject matter including an additional cell that is used as a reference during the differential sensing.

210.11 Compensate signal:
Subject matter under subclass 210.1 wherein the output signal from an additional (reference) circuit is used to offset undesired voltage variations.

210.12 Voltage setting:
Subject matter under subclass 210.1 wherein a reference voltage is selected according to storage levels or operation modes.

210.13 Common bit line:
Subject matter under subclass 210.1 wherein a reference cell shares the same bit/data line with a storage element.

210.14 Plural elements per reference cell:
Subject matter under subclass 210.1 wherein a reference cell has more than one electronic components (e.g., containing a combination of transistors, capacitors, resistors, fuse, etc.).

210.15 Structural component of a reference cell:
Subject matter under subclass 210.1 Including the structure of the electronic component (e.g., transistor, resistor, capacitor, fuse, etc.) that makes up a reference cell.

233.1 Sync/clocking
This subclass is intended under subclass 230.01. Subject matter where a circuit that generates a clock signal for controlling a memory cell and/or a circuit that makes a clock cycle occurring in a predetermined time sequence or in phase, is used to select a memory location.

233.11 Plural clock signals:
Subject matter under subclass 233.1 where there are two or more clock signals.

233.12 External clock signal modification:
Subject matter under subclass 233.1 wherein an external clock signal is adjusted.

233.13 DDR (double data rate) memory:
Subject matter under subclass 233.1 wherein a data memory reads or writes on a low to high transition of a clock signal and an opposite transition.

D. CHANGES TO THE DEFINITIONS

233.14 Initiating signal:
Subject matter under subclass 233.1 wherein a signal is used for activating an operational mode.

233.15 Standby signal:
Subject matter under subclass 233.1 wherein a clock signal is used for initiating a pause or power down mode.

233.16 Write mode signal only:
Subject matter under subclass 233.1 wherein a clock signal is used to control or start a write operation only.

233.17 Read mode signal only:
Subject matter under subclass 233.1 wherein a clock signal is used to control or start a read operation only.

233.18 Burst mode signal:
Subject matter under subclass 233.1 wherein a clock signal is used for transferring a group of data.

233.19 Common read and write mode signal:
Subject matter under subclass 233.1 wherein a clock signal is used to control or start both read and write operation.

D. CHANGES TO THE DEFINITIONS

CLASS 369 – DYNAMIC INFORMATION STORAGE OR RETRIEVAL

Subclass 47.32: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, appropriate subclasses for a type of static memory, particularly subclasses 189.01 through 225.7 for read or write circuitry.

Insert:

365, Static Information Storage and Retrieval, appropriate subclasses for a type of static memory, particularly subclasses 189.011 through 225.7 for read or write circuitry.

D. CHANGES TO THE DEFINITIONS

CLASS 370 – MULTIPLEX COMMUNICATIONS

Class Definition: Section II, under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01+ and 230.01+, for a static memory system with the handling of signal information or the addressing of memory locations respectively analogous to multiplexing techniques particularly subclasses 189.02 and 230.02 for such a system having multiplexed signals in each of the respective systems.

Insert:

365, Static Information Storage and Retrieval, subclasses 189.011 and 230.01+, for a static memory system with the handling of signal information or the addressing of memory locations respectively analogous to multiplexing techniques particularly subclasses 189.02 and 230.02 for such a system having multiplexed signals in each of the respective systems.

Subclass 395.7: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01 through 225.7 for read/write circuits in static information storage and retrieval.

Insert:

365, Static Information Storage and Retrieval, subclasses 189.011 through 225.7 for read/write circuits in static information storage and retrieval.

D. CHANGES TO THE DEFINITIONS

CLASS 375 – PULSE OR DIGITAL COMMUNICATIONS

Class Definition: Section III, under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01+ and 230.01+ for a read/write or addressing circuit which uses pulse signals in a static storage system

Insert:

365, Static Information Storage and Retrieval, subclasses 189.011 and 230.01+ for a read/write or addressing circuit which uses pulse signals in a static storage system

D. CHANGES TO THE DEFINITIONS

CLASS 711 – ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS:MEMORY

Class Definition: Section II, under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, various subclasses for static memory devices including internal elements of the memory, particularly subclasses 189.01+ for read/write circuits and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements; subclass 189.05 for buffering or latching data being read from or written to memory; subclass 189.08 for logic devices in combination with memory systems; subclasses 200 and 201 for testing of memory systems; and subclass 230.08 for buffering and latching address data being employed to access memory.

Insert:

365, Static Information Storage and Retrieval, various subclasses for static memory devices including internal elements of the memory, particularly subclasses 189.011 for read/write circuits and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements; subclass 189.05 for buffering or latching data being read from or written to memory; subclass 189.08 for logic devices in combination with memory systems; subclasses 200 and 201 for testing of memory systems; and subclass 230.08 for buffering and latching address data being employed to access memory.

Subclass 1: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01+ for read/write circuits, and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements of the same type.

Insert:

365, Static Information Storage and Retrieval, subclasses 189.011 for read/write circuits, and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements of the same type.

D. CHANGES TO THE DEFINITIONS

Subclass 3: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 49+ for internal aspects of associative memory.

Insert:

365, Static Information Storage and Retrieval, subclasses 49.1 for internal aspects of associative memory.

Subclass 102: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, appropriate subclasses for storage having a particular internal cell structure (e.g., subclass 94 for read only (i.e., semipermanent) systems), subclasses 189.01+ for memory read/write circuits, and subclasses 230.01+ for addressing circuits

Insert:

365, Static Information Storage and Retrieval, appropriate subclasses for storage having a particular internal cell structure (e.g., subclass 94 for read only (i.e., semipermanent) systems), subclasses 189.011 for memory read/write circuits, and subclasses 230.01+ for addressing circuits

Subclass 108: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 49 and 50 for associative memories or content addressable memories (CAM), per se.

Insert:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories or content addressable memories (CAM), per se.

Subclass 113: Under SEE OR SEARCH CLASS

Delete:

D. CHANGES TO THE DEFINITIONS

365, Static Information Storage and Retrieval, subclasses 49 and 50 for associative memories and caches under their class definition.

Insert:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories and caches under their class definition.

Subclass 118: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 49 and 50 for associative memories and caches at the cell level.

Insert:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories and caches at the cell level.

Subclass 128: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 49+ for associative memories or content addressable memories (CAM), per se.

Insert:

365, Static Information Storage and Retrieval, subclasses 49.1 through 50 for associative memories or content addressable memories (CAM), per se.

Subclass 200: Under SEE OR SEARCH CLASS

Delete:

365, Static Information Storage and Retrieval, subclasses 189.01+ for read/write circuits and subclasses 230.01+ for addressing of addressable, static single storage elements or plural elements of the same type.

Insert:

365, Static Information Storage and Retrieval, subclasses 189.011 for read/write circuits and subclasses 230.01+ for addressing of

D. CHANGES TO THE DEFINITIONS

addressable, static single storage elements or plural elements of the same type.